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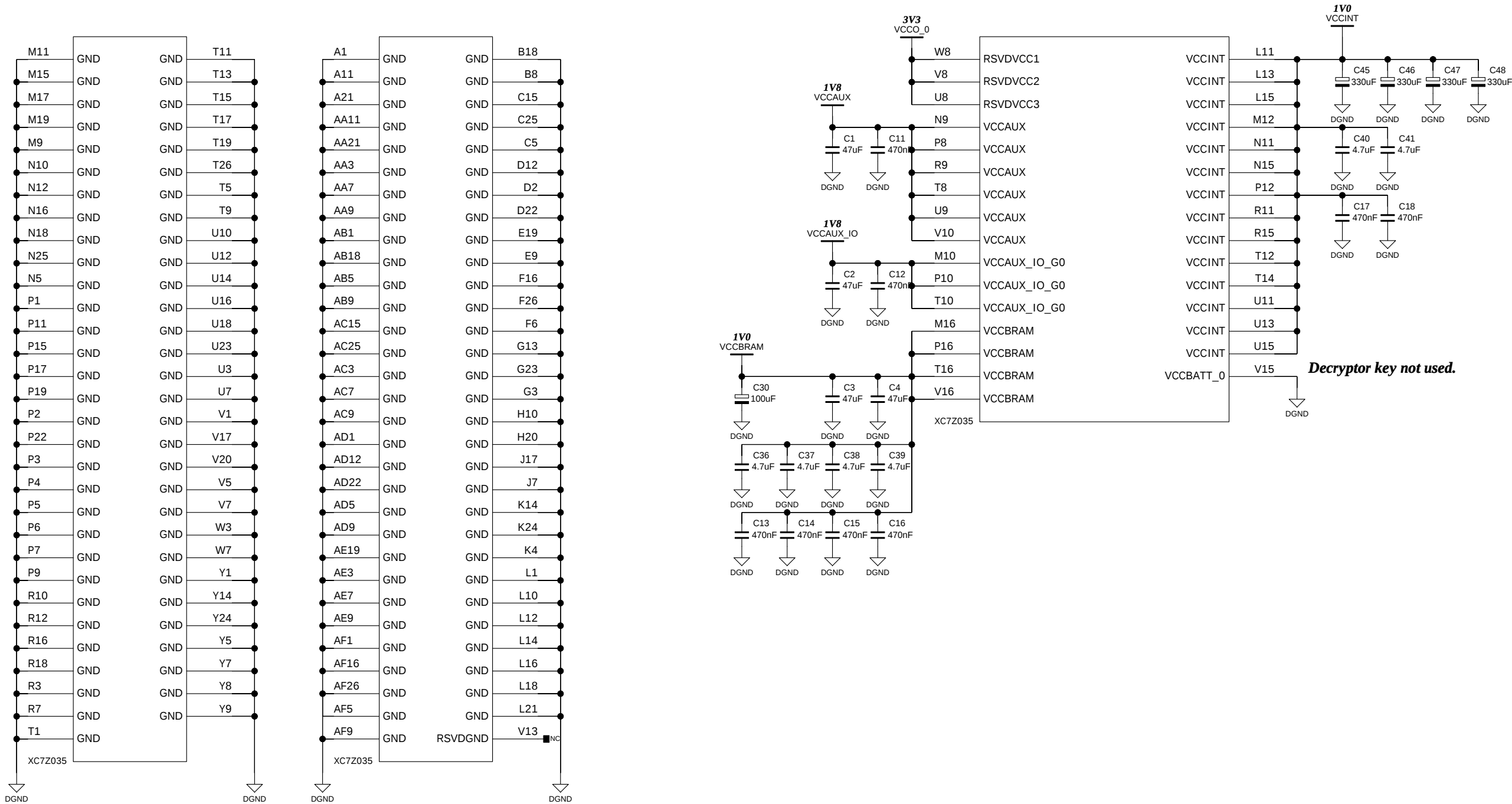
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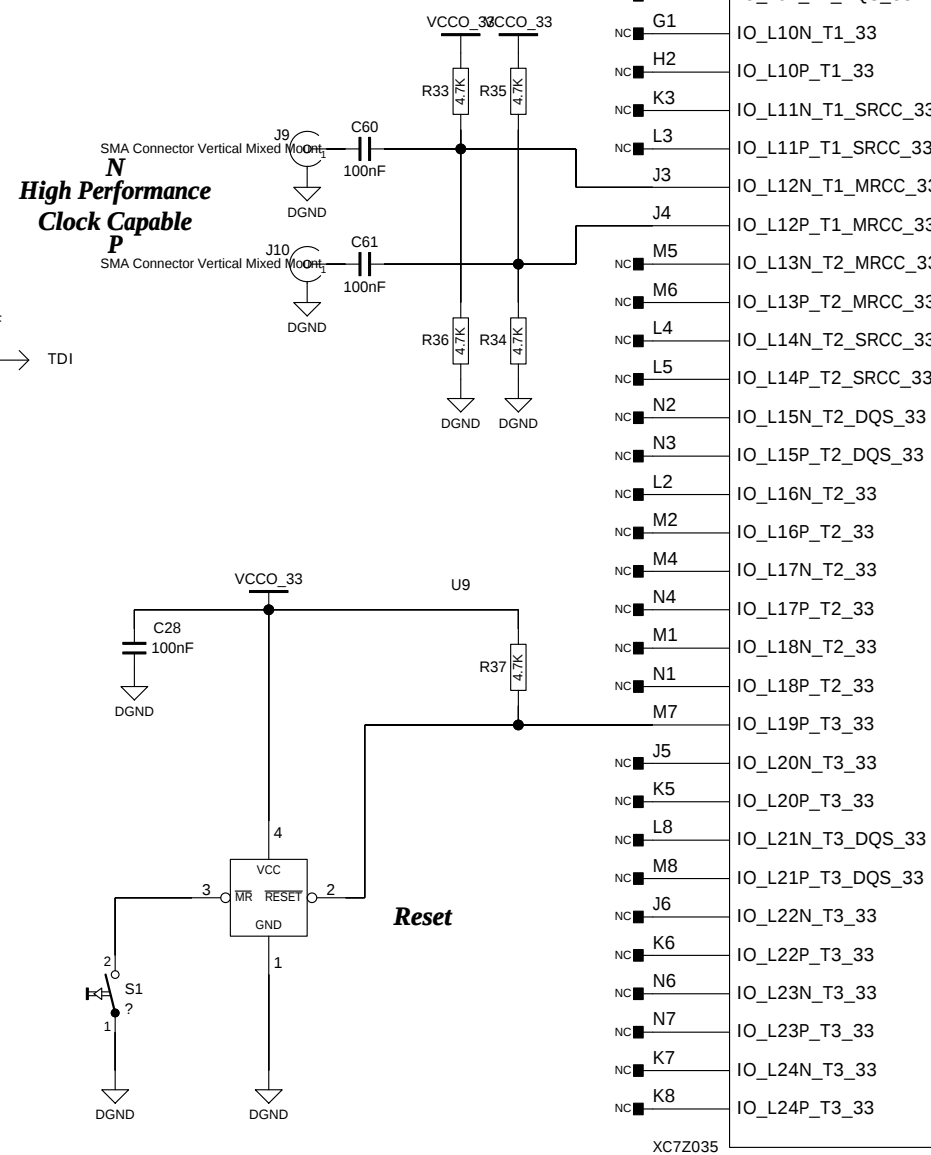
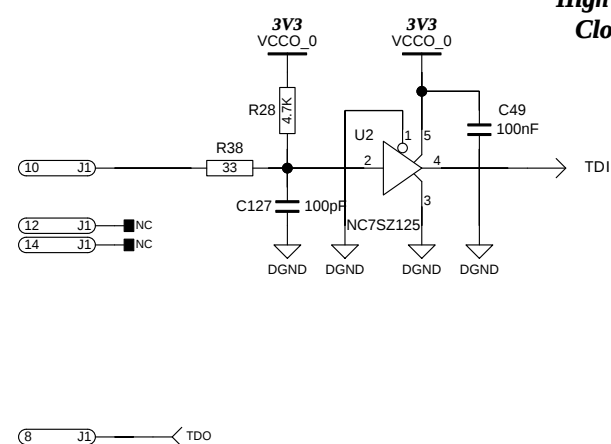
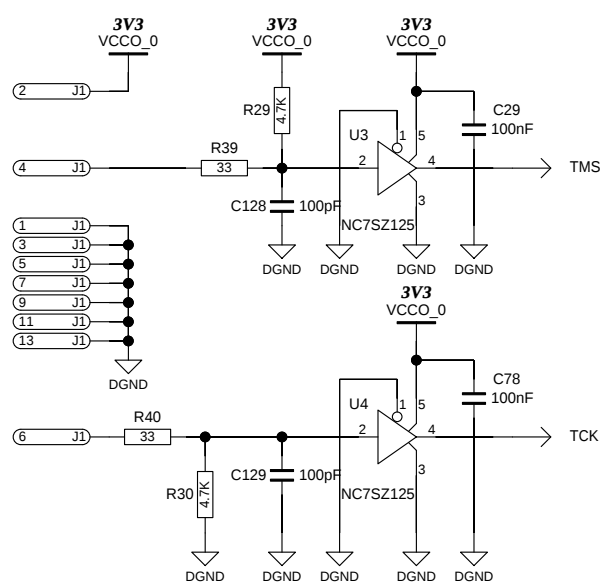
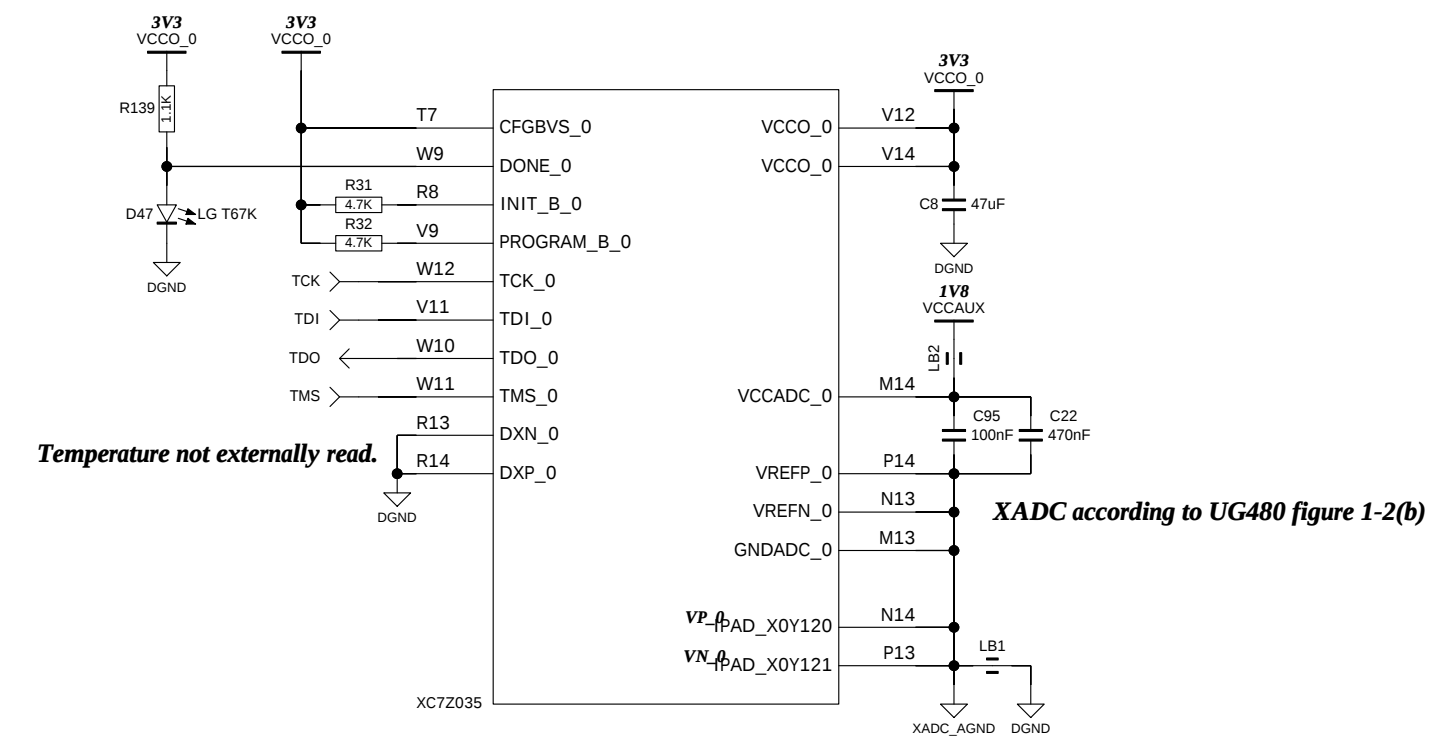
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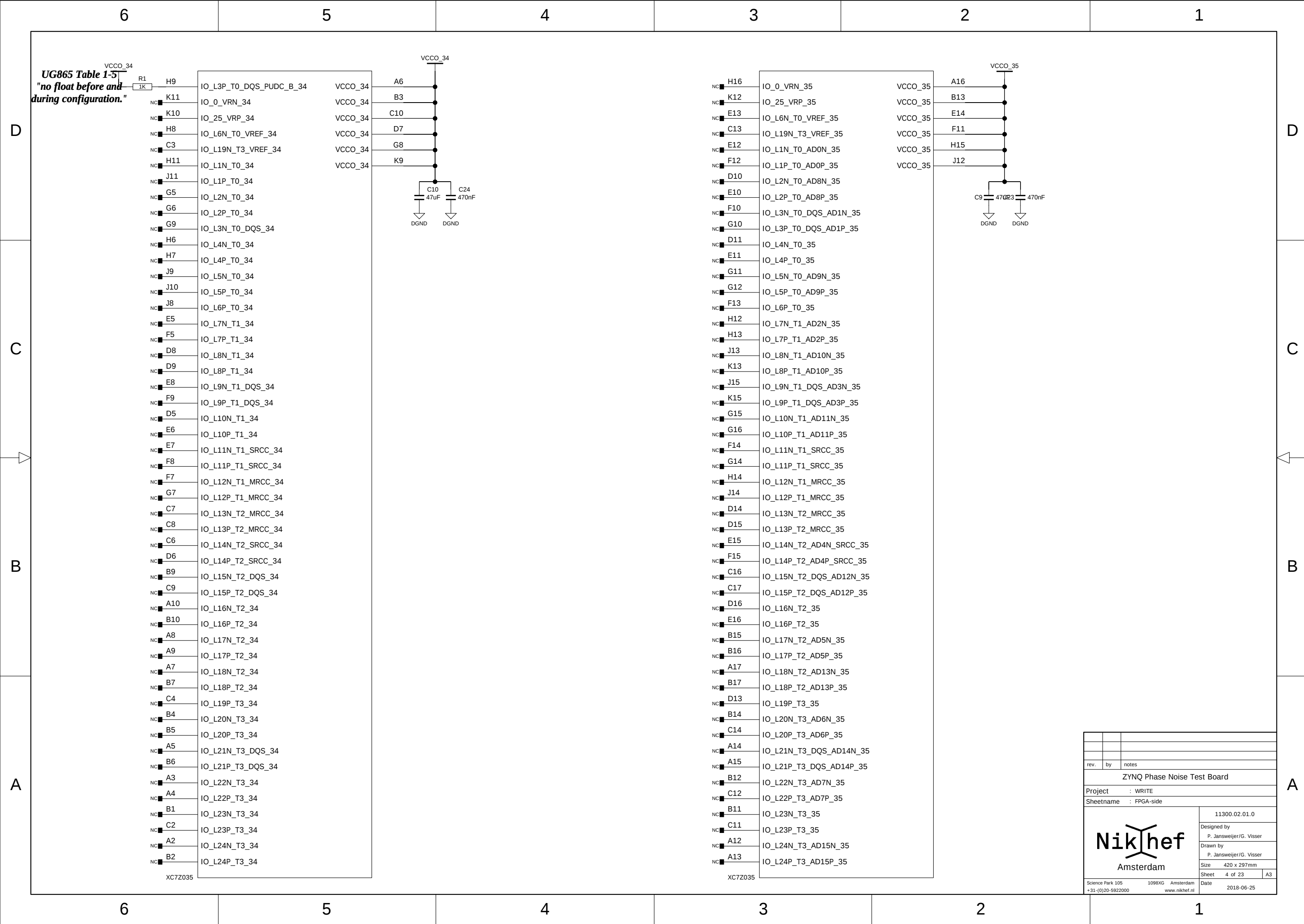
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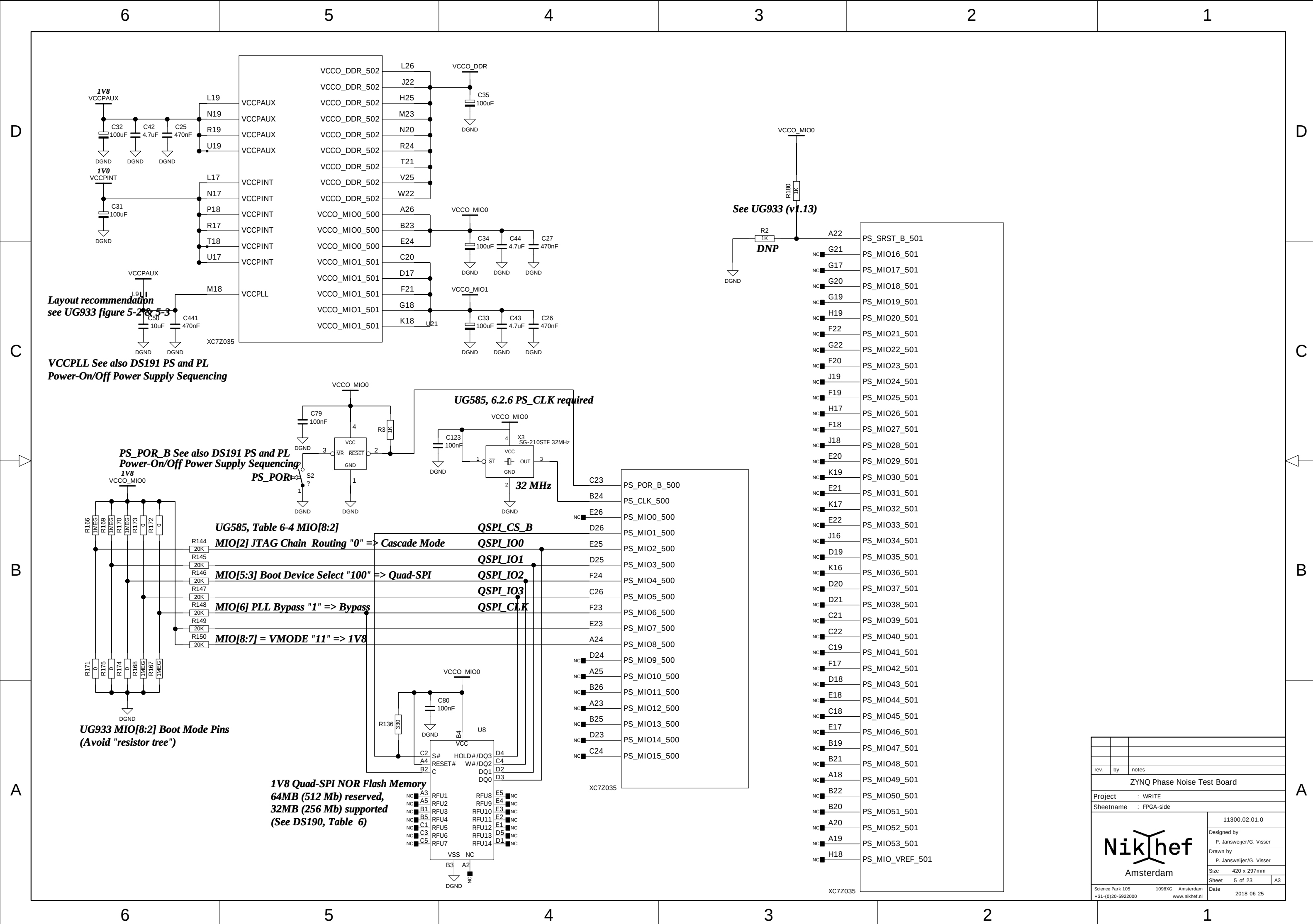


rev.	by	notes
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Project : WRITE		
Sheetname : FPGA-side		
		11300.02.01.0
		Designed by P. Jansweijer/G. Visser
		Drawn by P. Jansweijer/G. Visser
		Size 420 x 297mm
		Sheet 1 of 23 A3
Science Park 105 +31-(0)20-5922000	1098XG Amsterdam www.nikhef.nl	Date 2018-06-25



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ZYNQ Phase Noise Test Board			
Project	: WRITE		
Sheetname	: FPGA-side		
			11300.02.01.0
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			P. Jansweijer/G. Visser
			Drawn by
			P. Jansweijer/G. Visser
			Size
Sheet	3 of 23	A	
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Date	2018-06-25		





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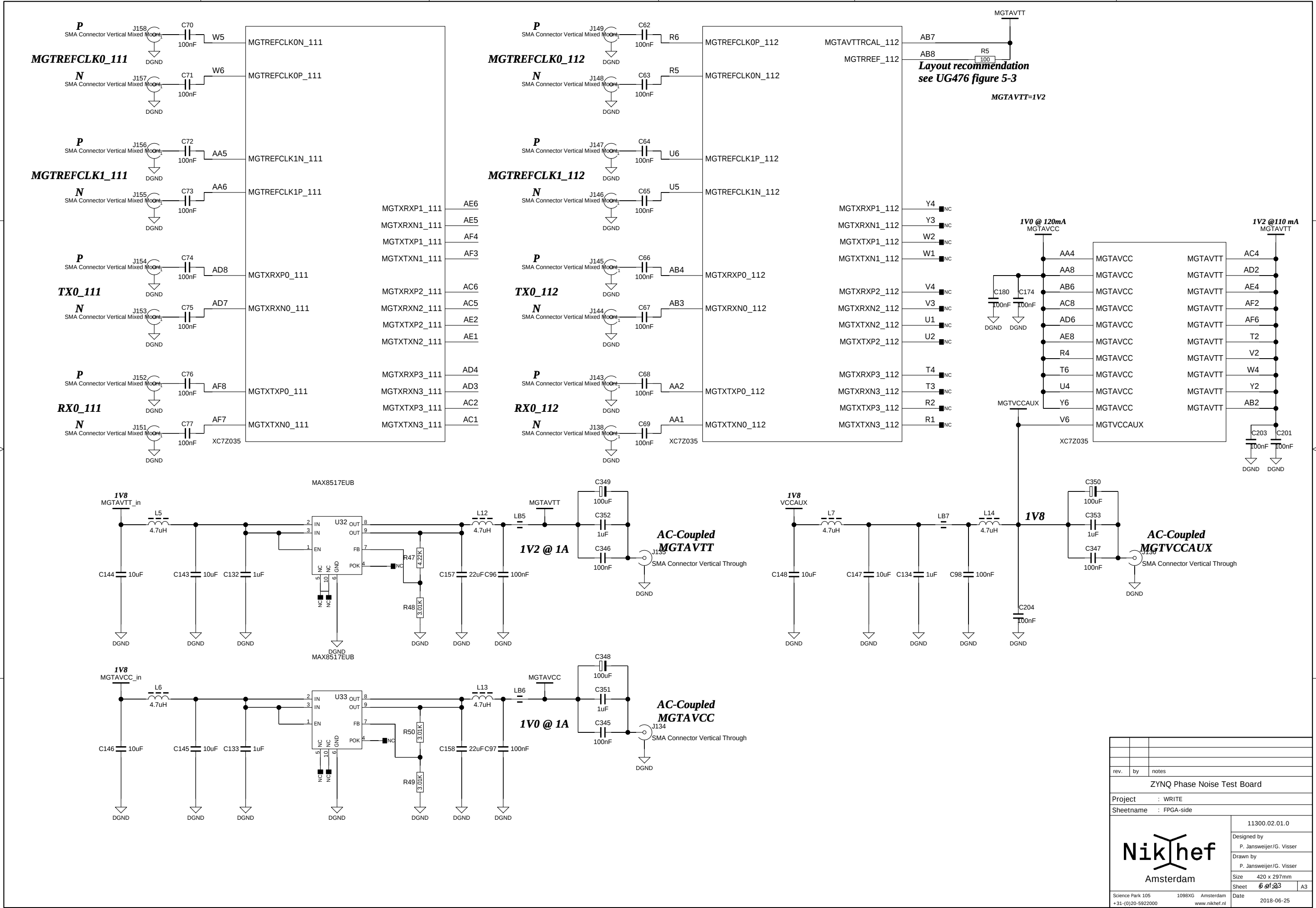
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		Drawn by P. Jansweijer/G. Visser
		Size 420 x 297mm
Science Park 105 +31-(0)20-5922000	1098XG Amsterdam www.nikhef.nl	Sheet 6 of 23 Date 2018-06-25

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ZYNQ Phase Noise Test Board		
Project : WRITE		
Sheetname : FPGA-side		
		11300.02.01.0
		Designed by P. Jansweijer/G. Visser
		Drawn by P. Jansweijer/G. Visser
		Size 420 x 297mm
		Sheet 7 of 23
		Date 2018-06-25
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Nikhet
Amsterdam

	11300.02.01.0
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Designed by	
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P. Jansweijer/G. Viss

P. Jansweijer/G. Viss

Size	420 x 297mm
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Sheet 7 of 23

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2018-06-25

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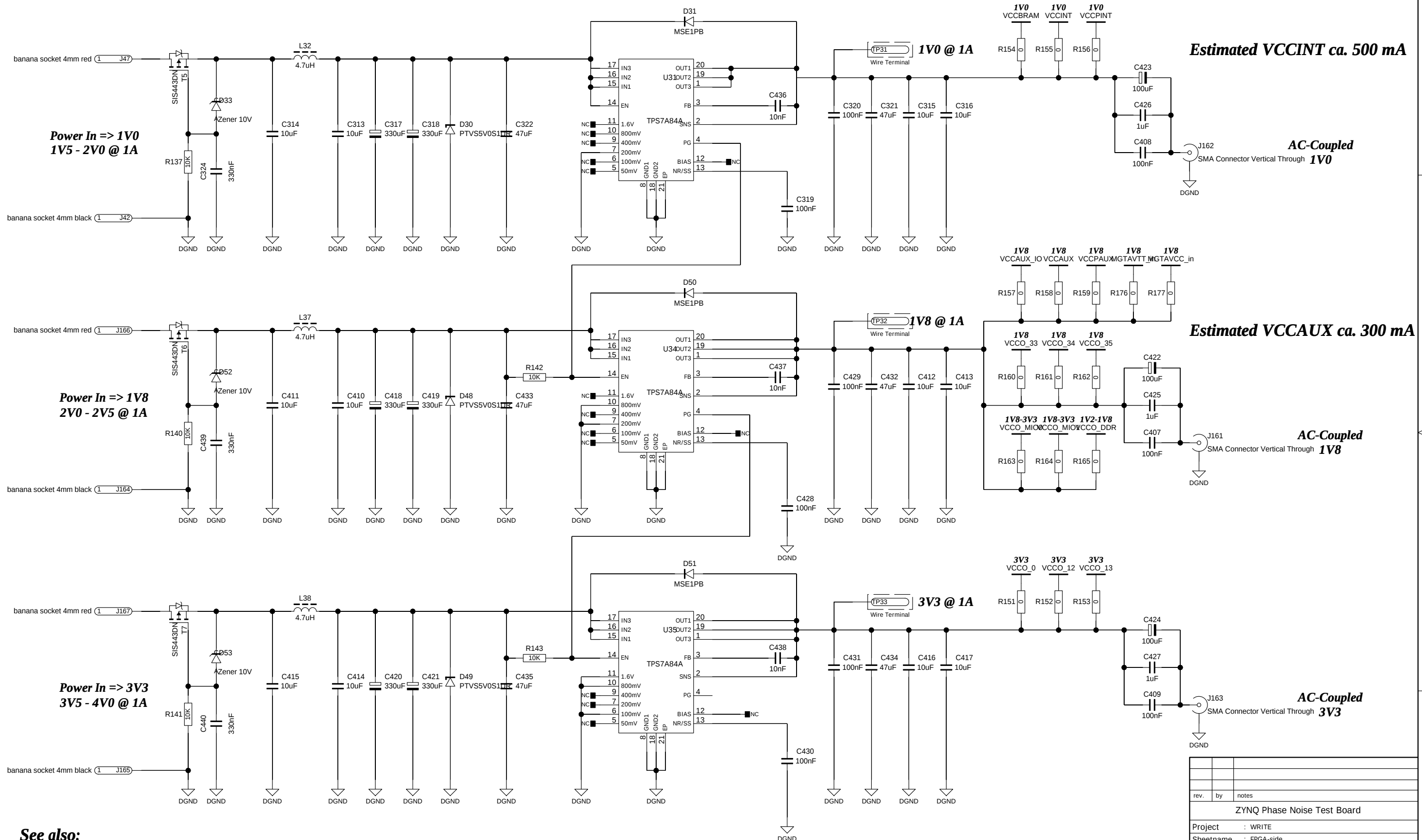
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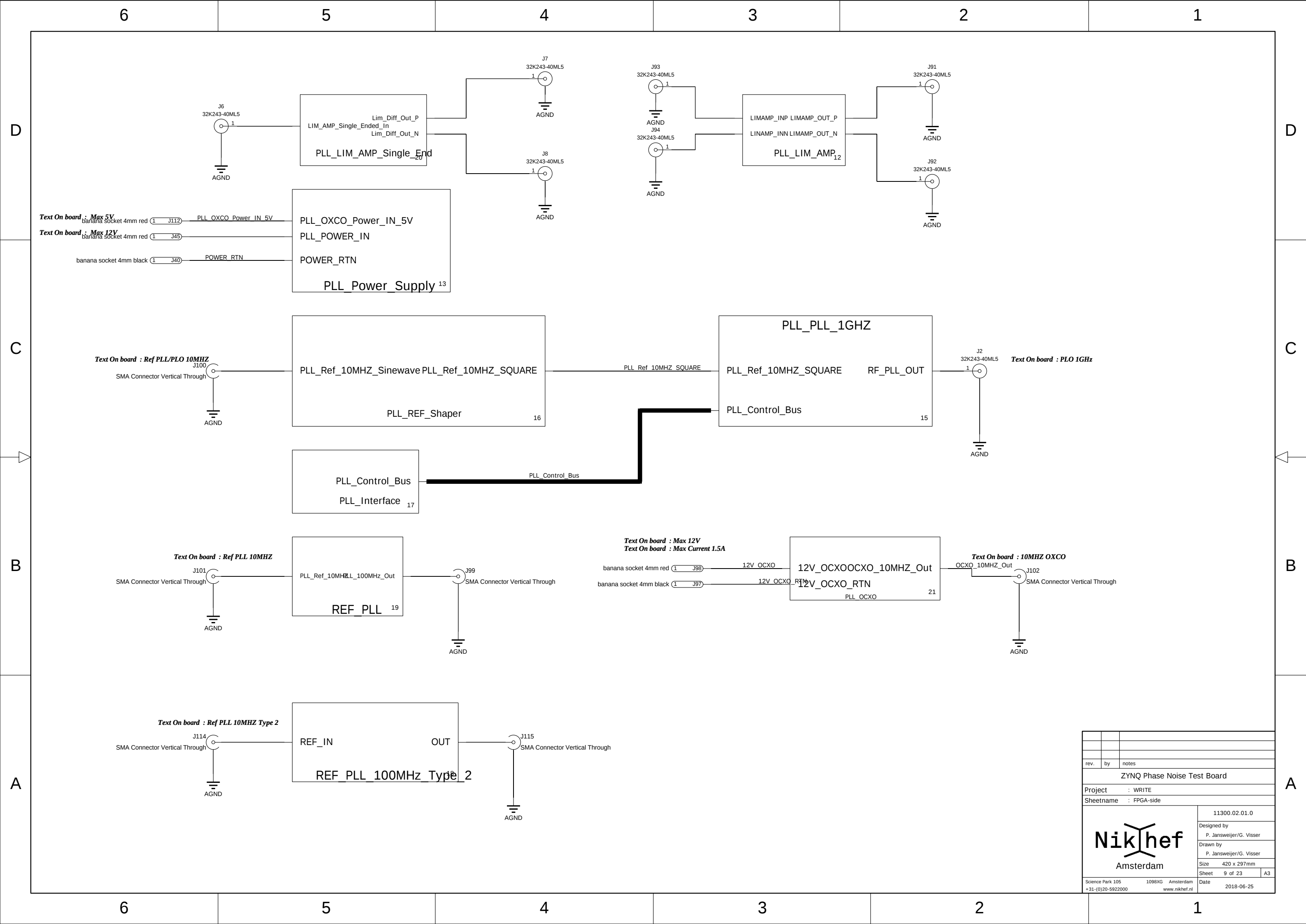
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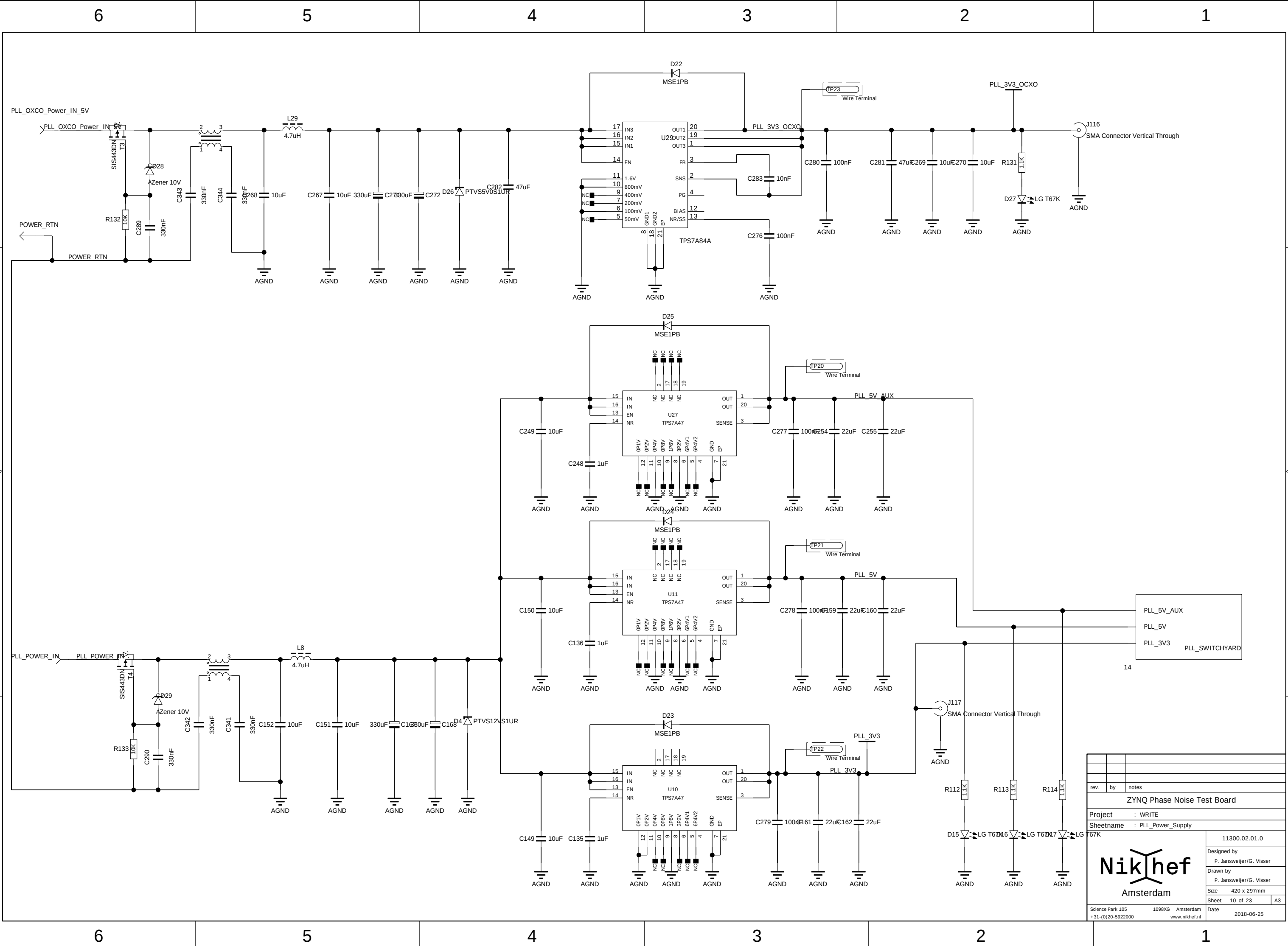


See also:
DS191 PS and PL Power-On/Off Power Supply Sequencing
On: 1V0 -> 1V8 -> 3V3

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ZYNQ Phase Noise Test Board		
Project : WRITE		
Sheetname : FPGA-side		
 Nikhef Amsterdam		11300.02.01.0
		Designed by P. Jansweijer/G. Visser
		Drawn by P. Jansweijer/G. Visser
		Size 420 x 297mm
		Sheet 8 of 23
		A3
Science Park 105 +31-(0)20-5922000		1098XG Amsterdam www.nikhef.nl
Date	2018-06-25	



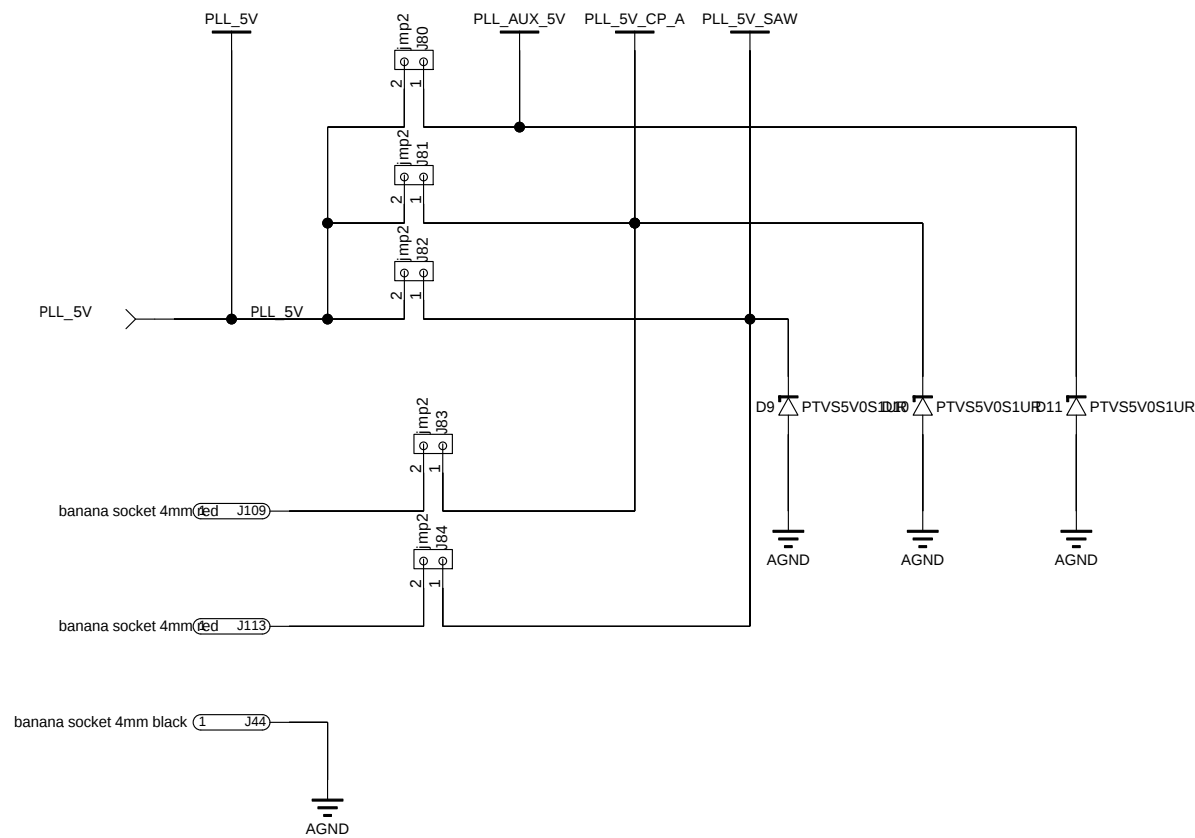
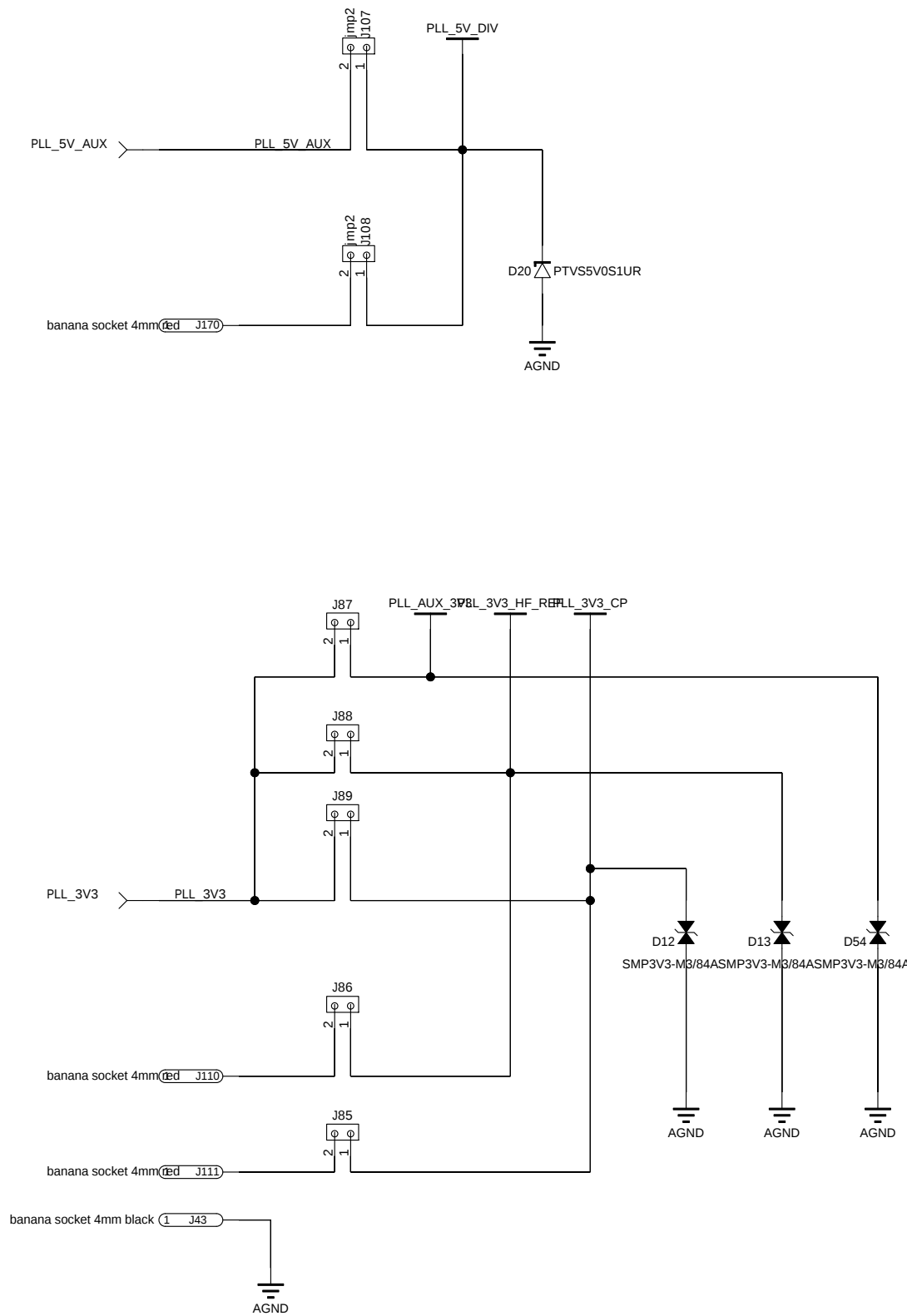
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Sheetname : FPGA-side		
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		Sheet 9 of 23 A3
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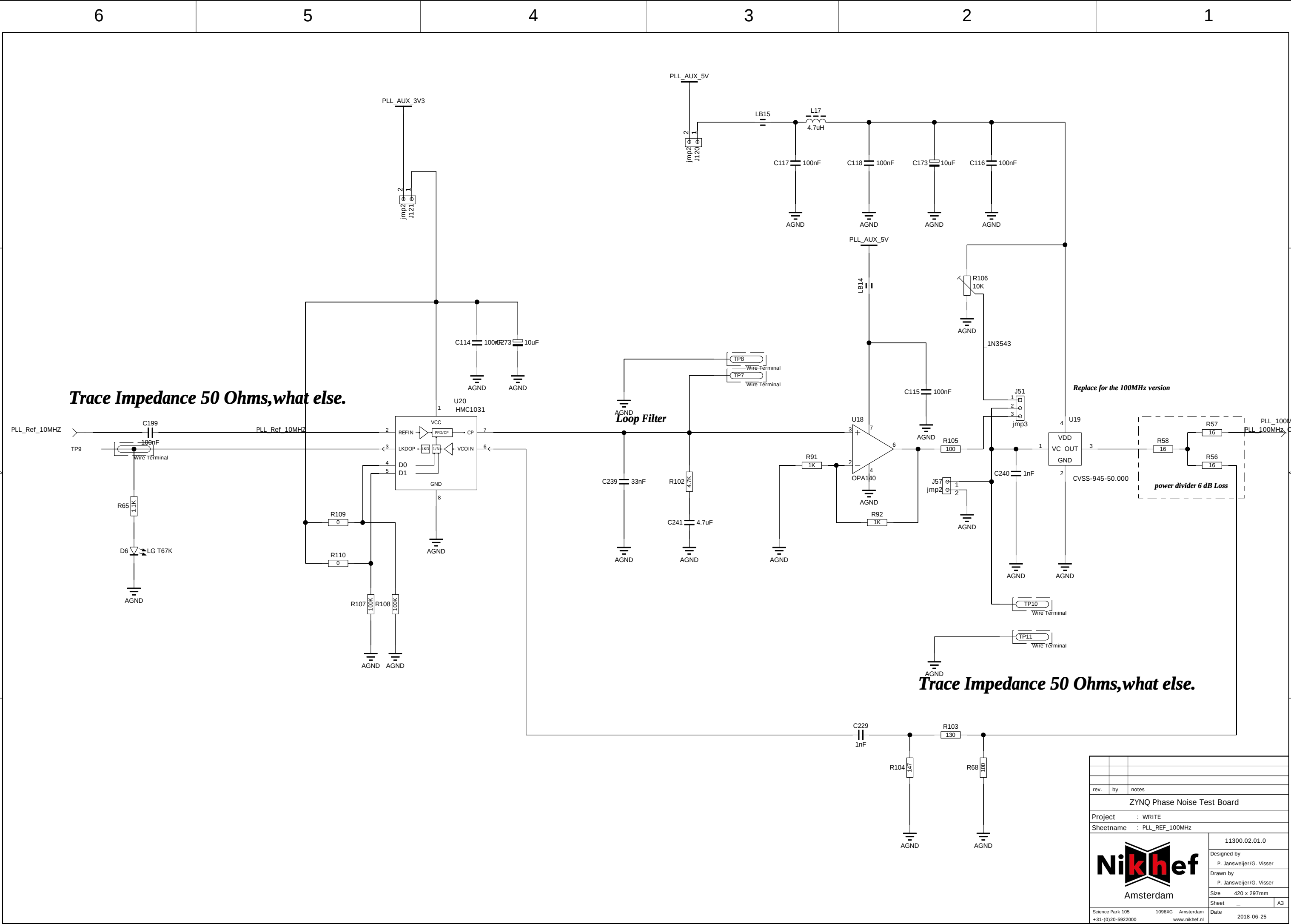
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11300.02.01.0		
Designed by		P. Jansweijer/G. Visser
Drawn by		P. Jansweijer/G. Visser
Size		420 x 297mm
Sheet		10 of 23
Date		2018-06-25
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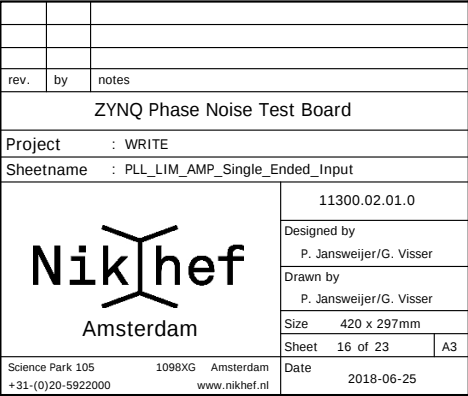
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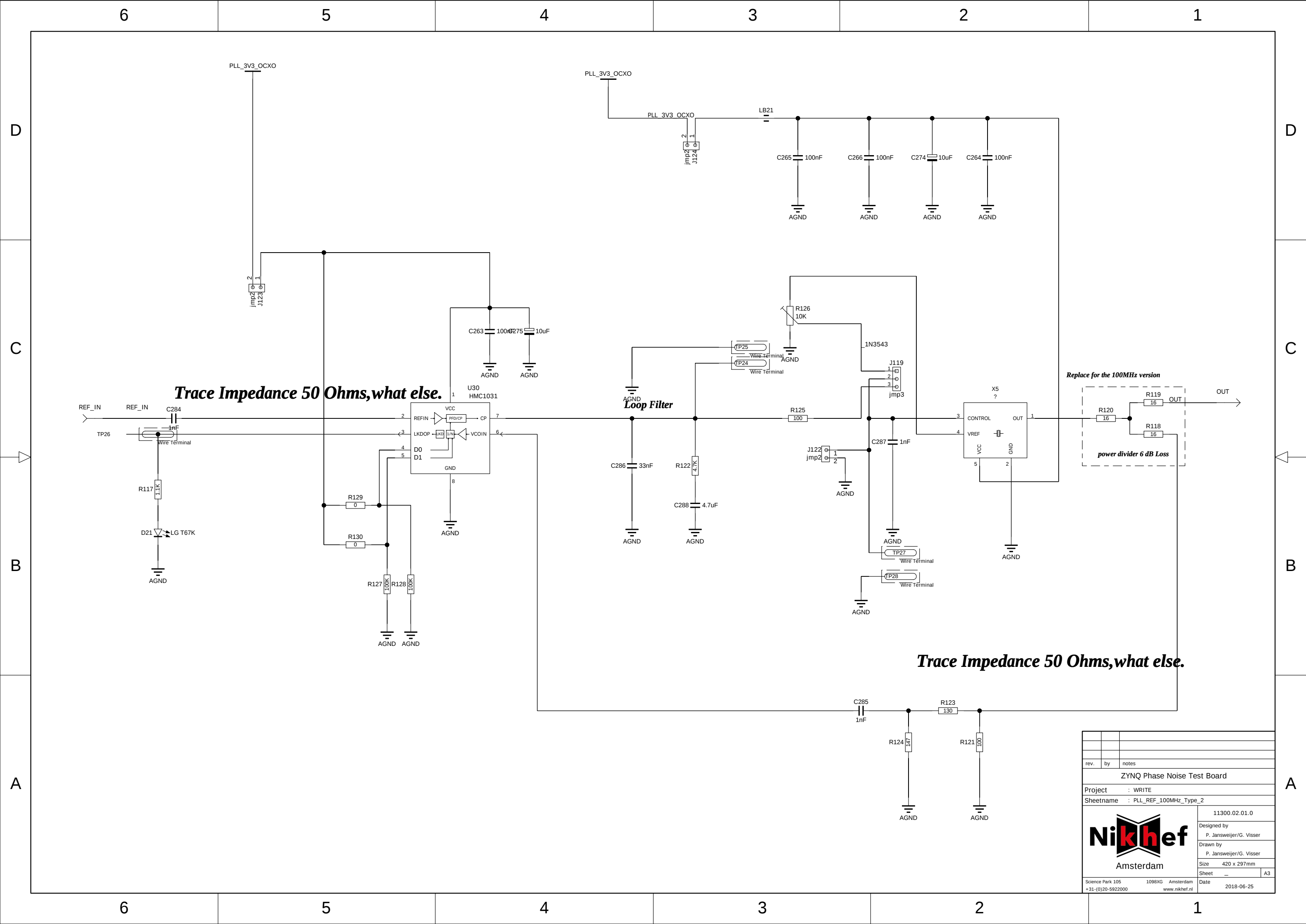


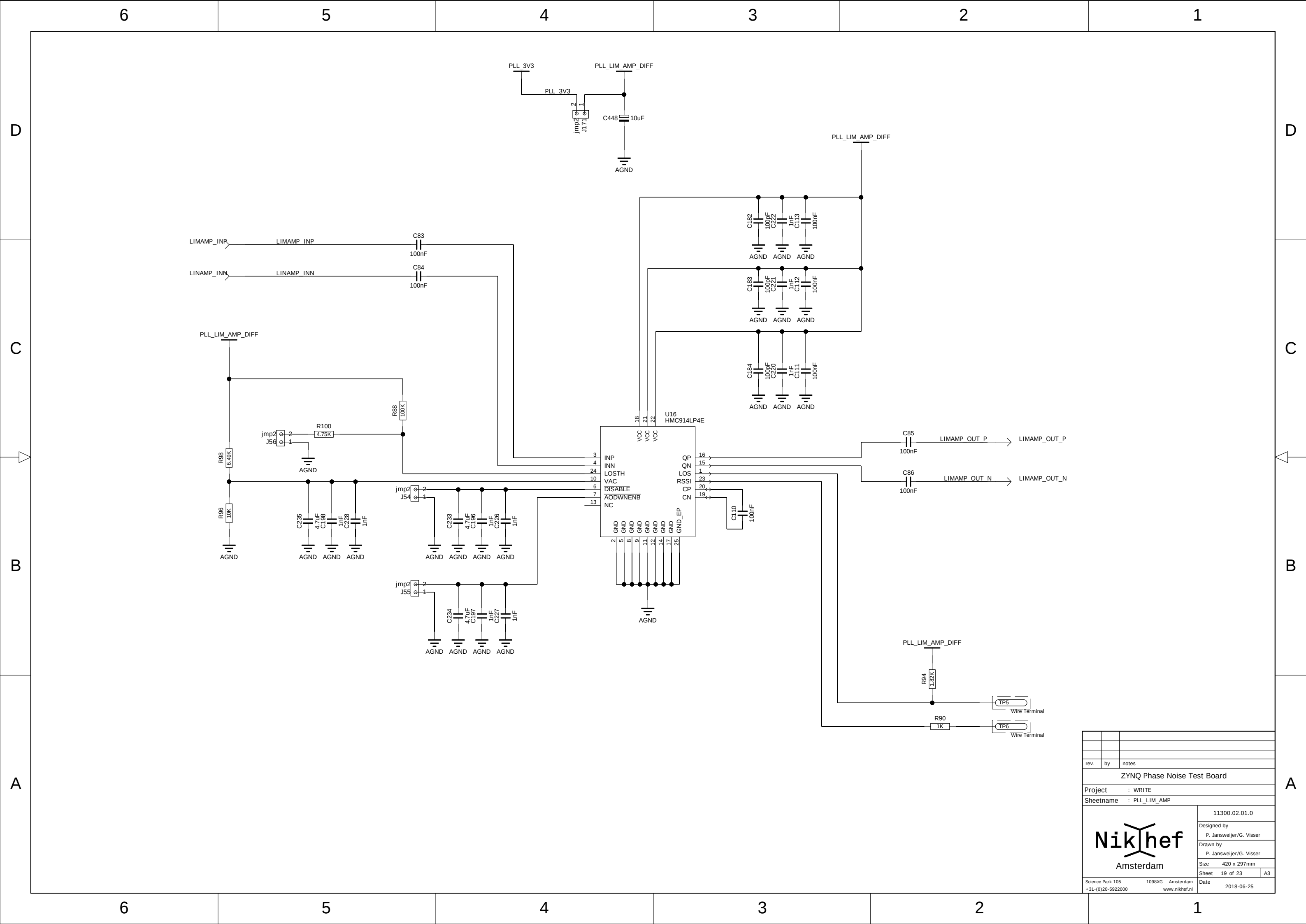
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		Size 420 x 297mm
		Sheet 11 of 23 A3
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ZYNQ Phase Noise Test Board		
Project	: WRITE	
Sheetname	: PLL_REF_100MHz	
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		Designed by P. Jansweijer/G. Visser
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		Size 420 x 297mm
Sheet	A3	
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ZYNQ Phase Noise Test Board		
Project : WRITE		
Sheetname : PLL_LIM_AMP		
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		Designed by P. Jansweijer/G. Visser
		Drawn by P. Jansweijer/G. Visser
		Size 420 x 297mm
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Sheet		19 of 23
		A3

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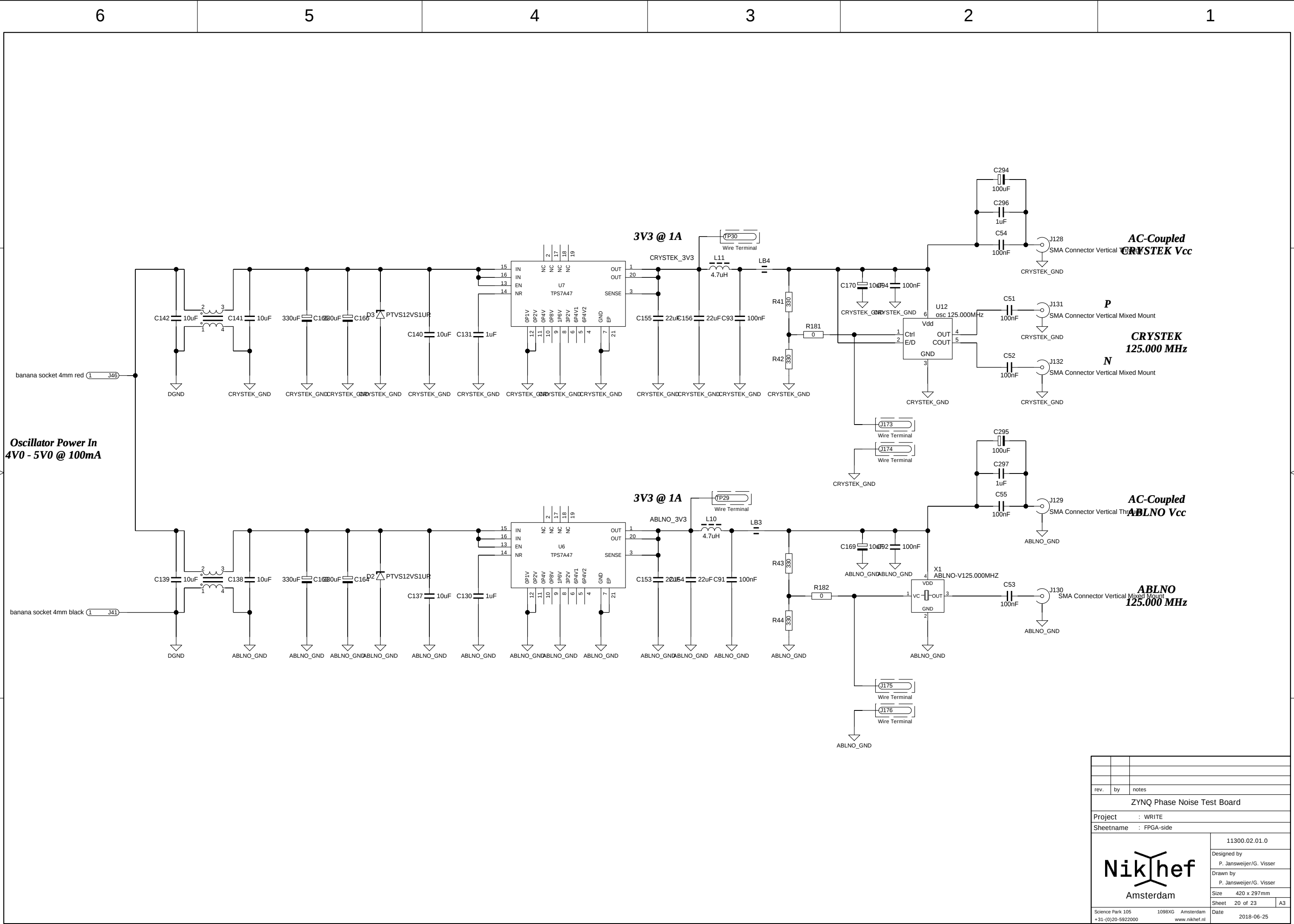
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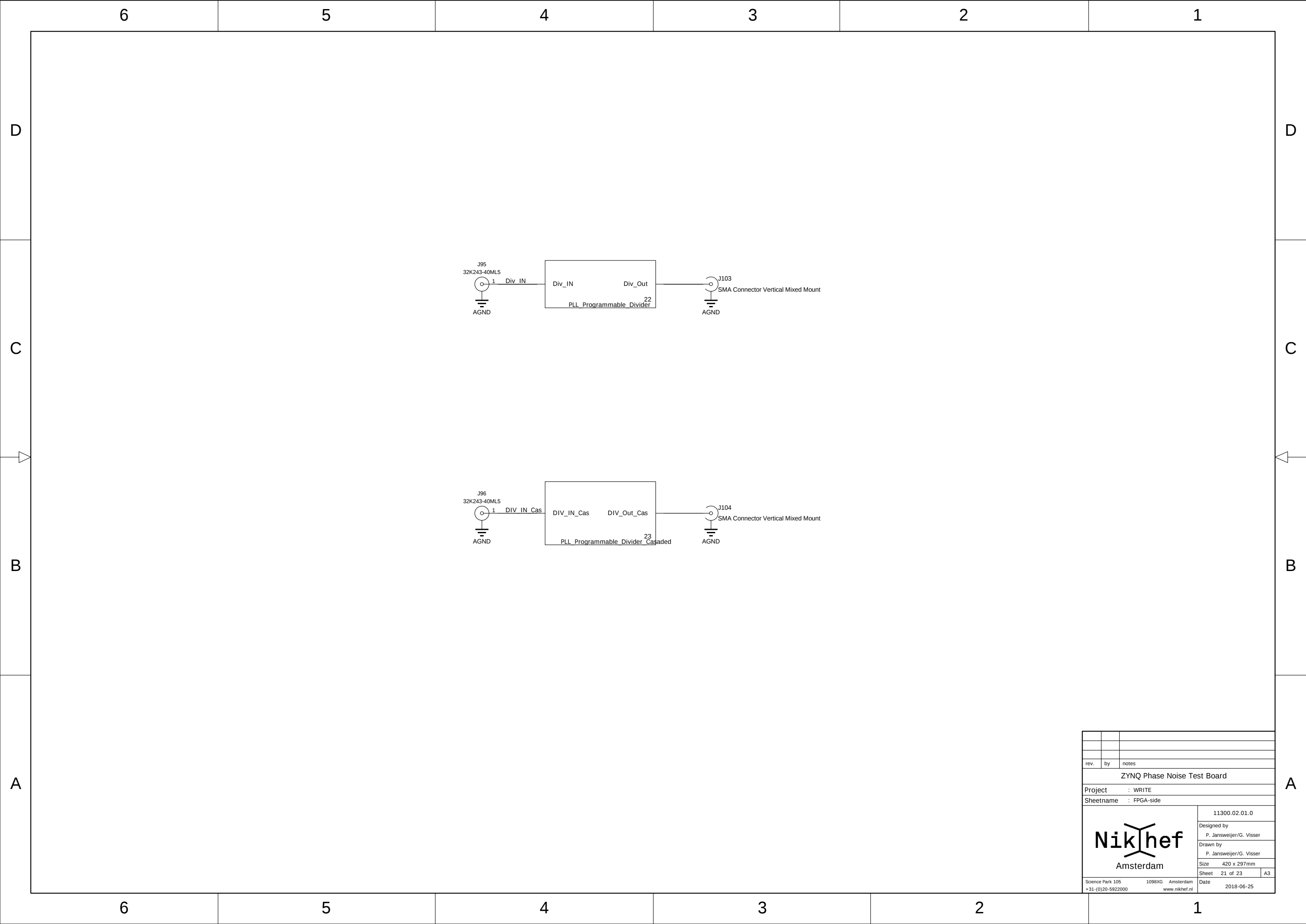
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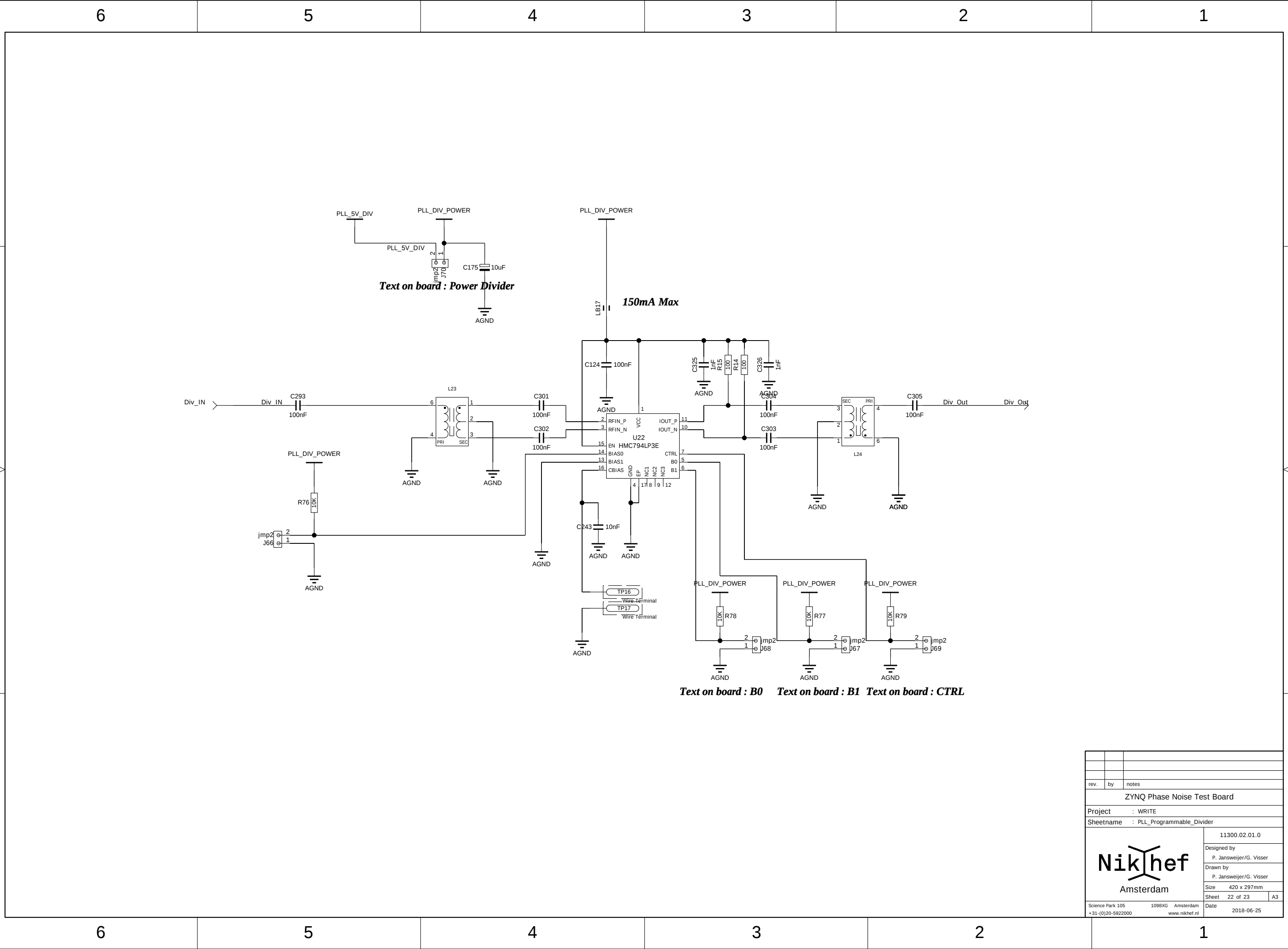
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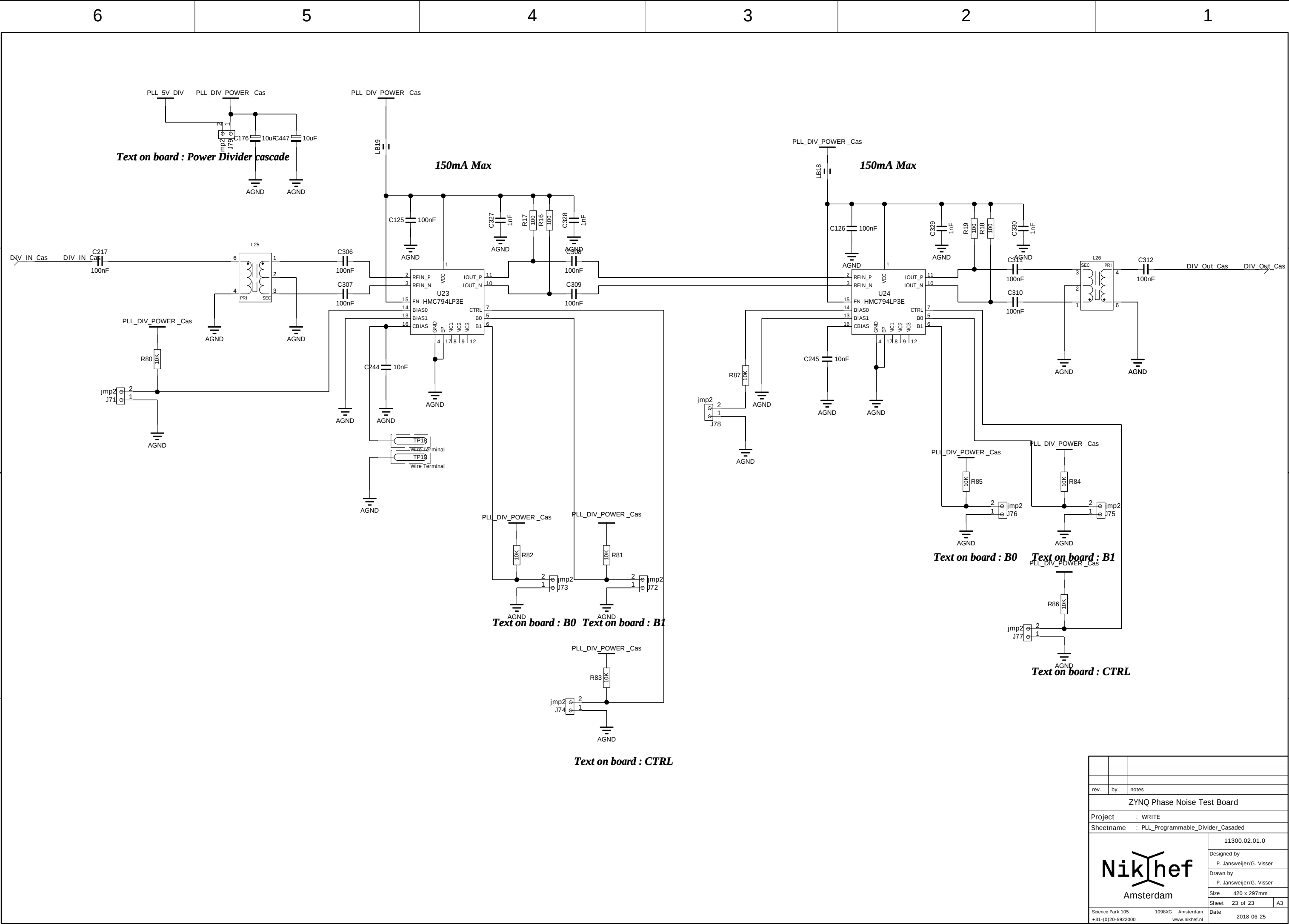


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		Drawn by P. Jansweijer/G. Visser
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		Sheet 20 of 23 A3
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Project : WRITE		
Sheetname : PLL_Programmable_Divider		
		11300.02.01.0
		Designed by P. Jansweijer/G. Visser
		Drawn by P. Jansweijer/G. Visser
		Size 420 x 297mm
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ZYNQ Phase Noise Test Board		
Project : WRITE		
Sheetname : PLL_Programmable_Divider_Casaded		
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		Designed by P. Jansweijer/G. Visser
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		Size 420 x 297mm
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