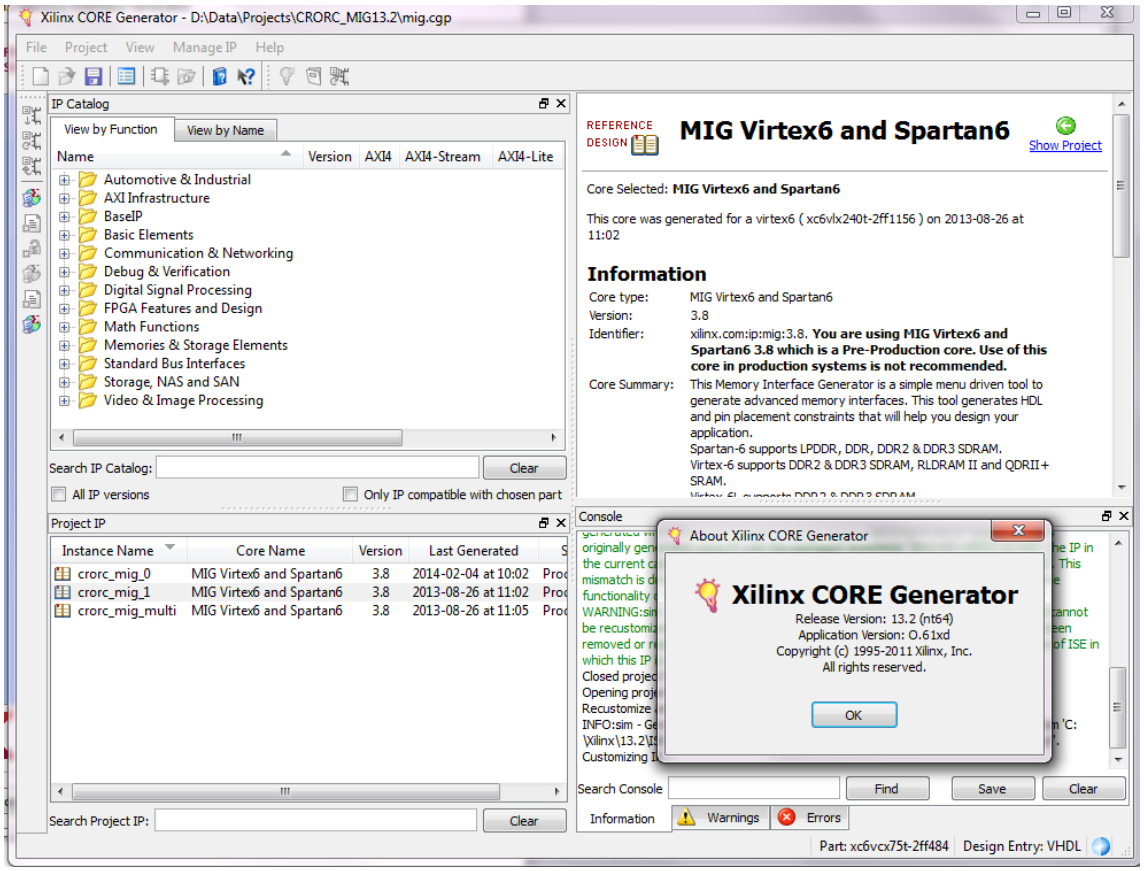
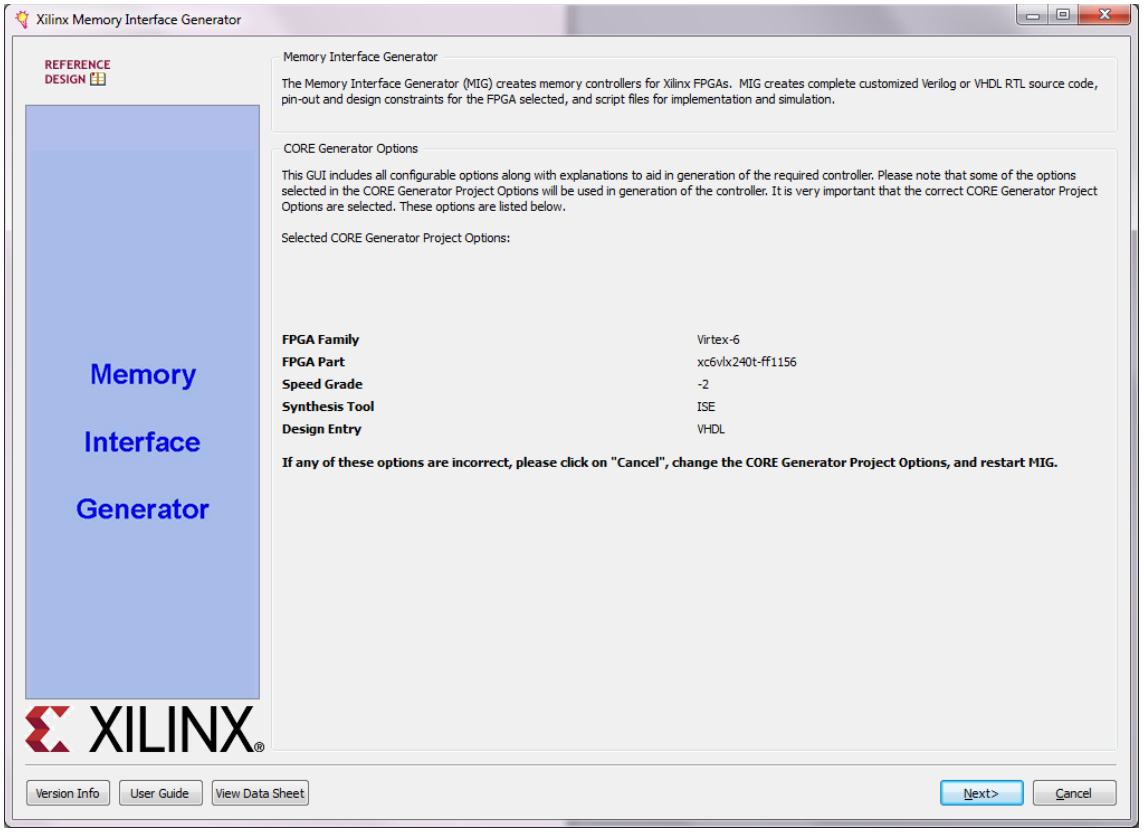
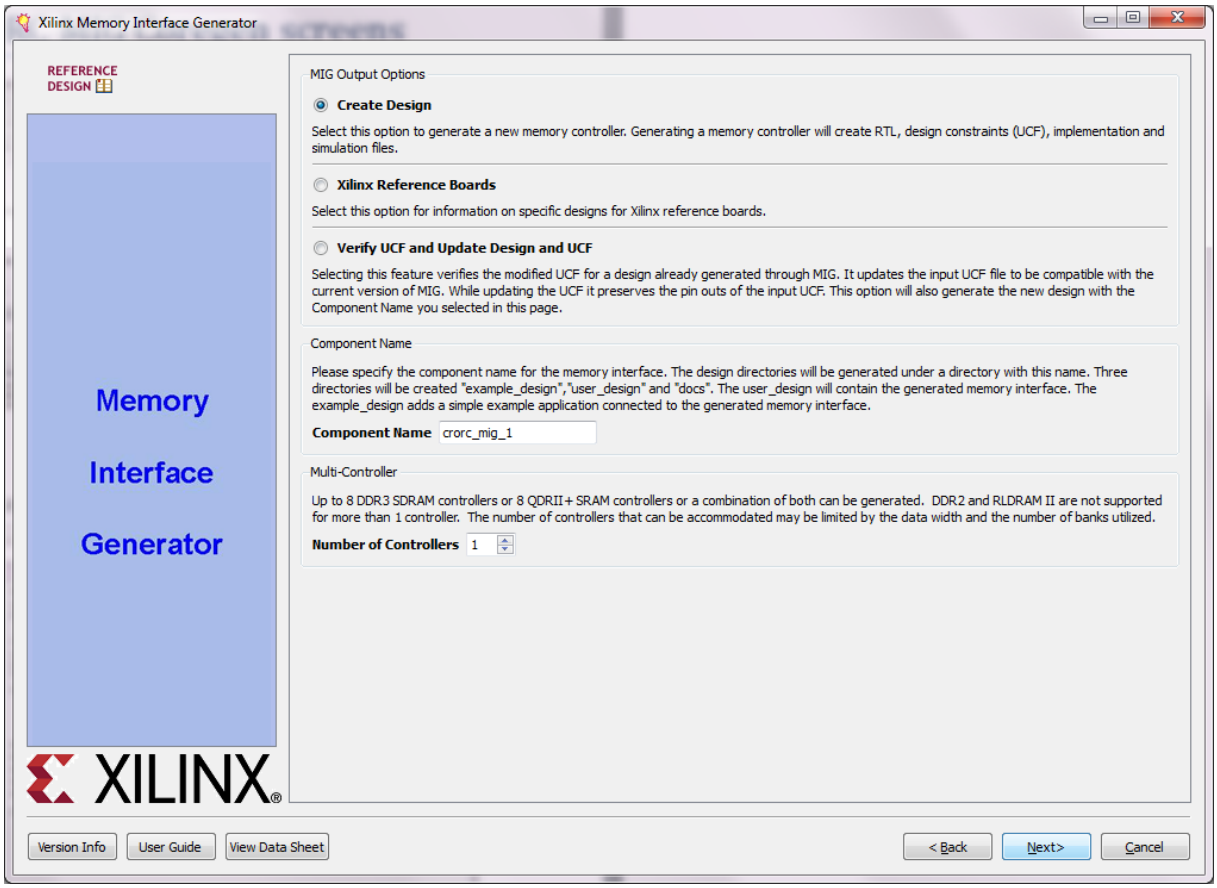
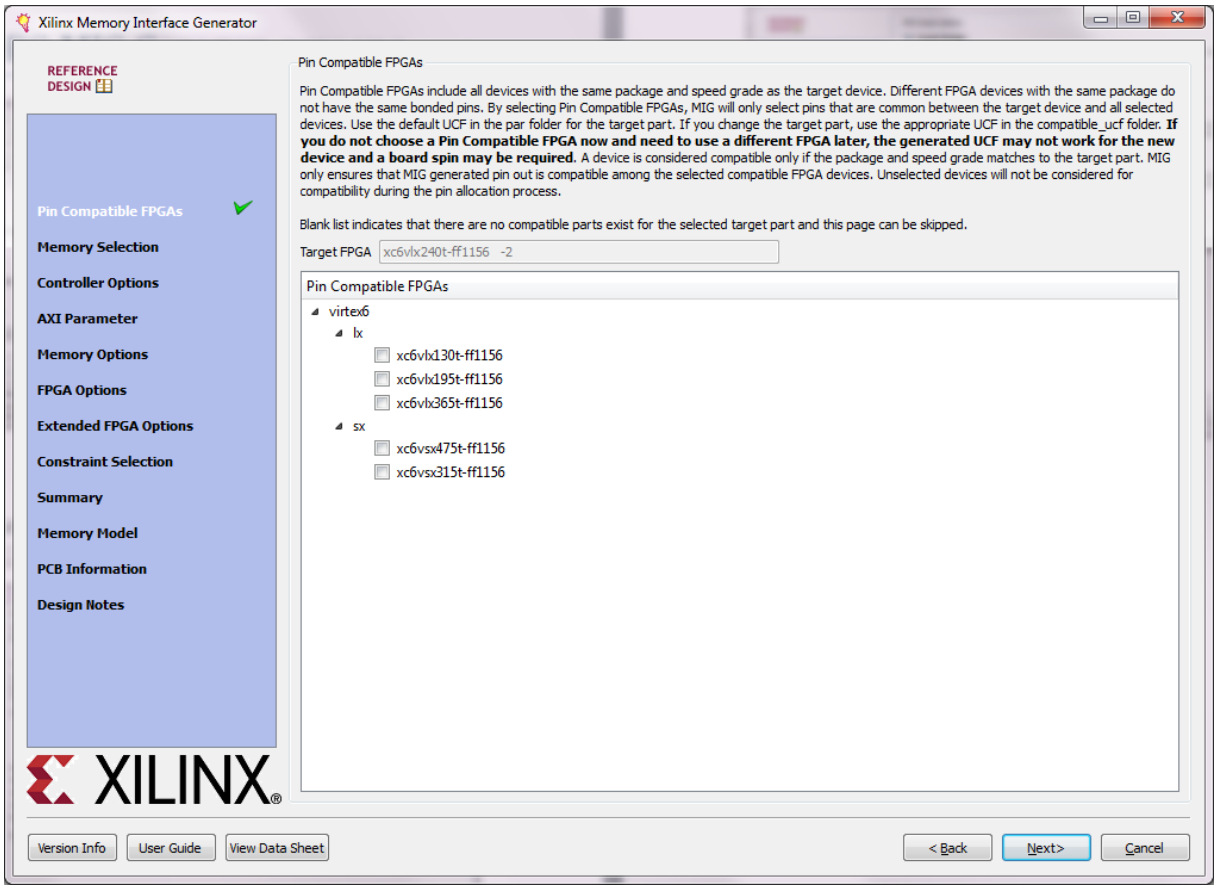
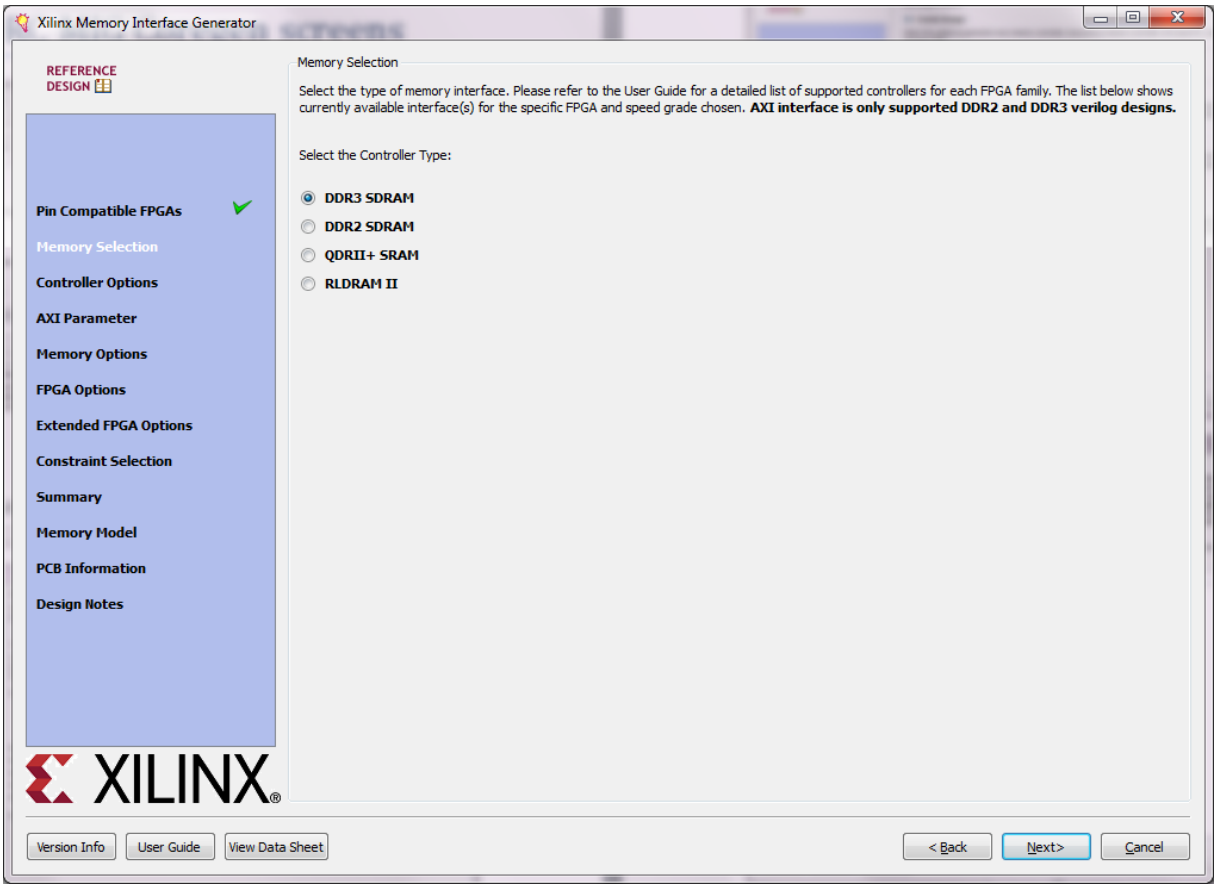
C-RORC MIG Coregen screens

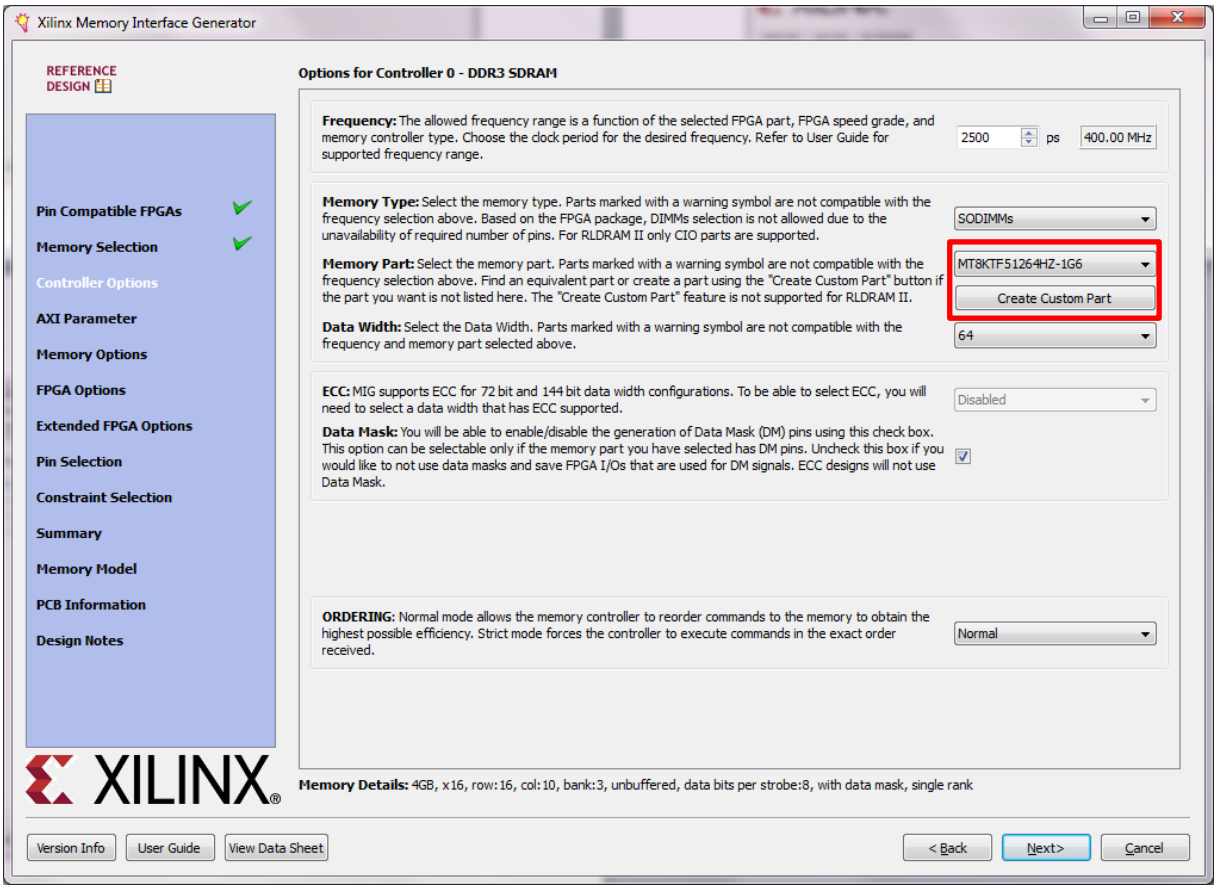


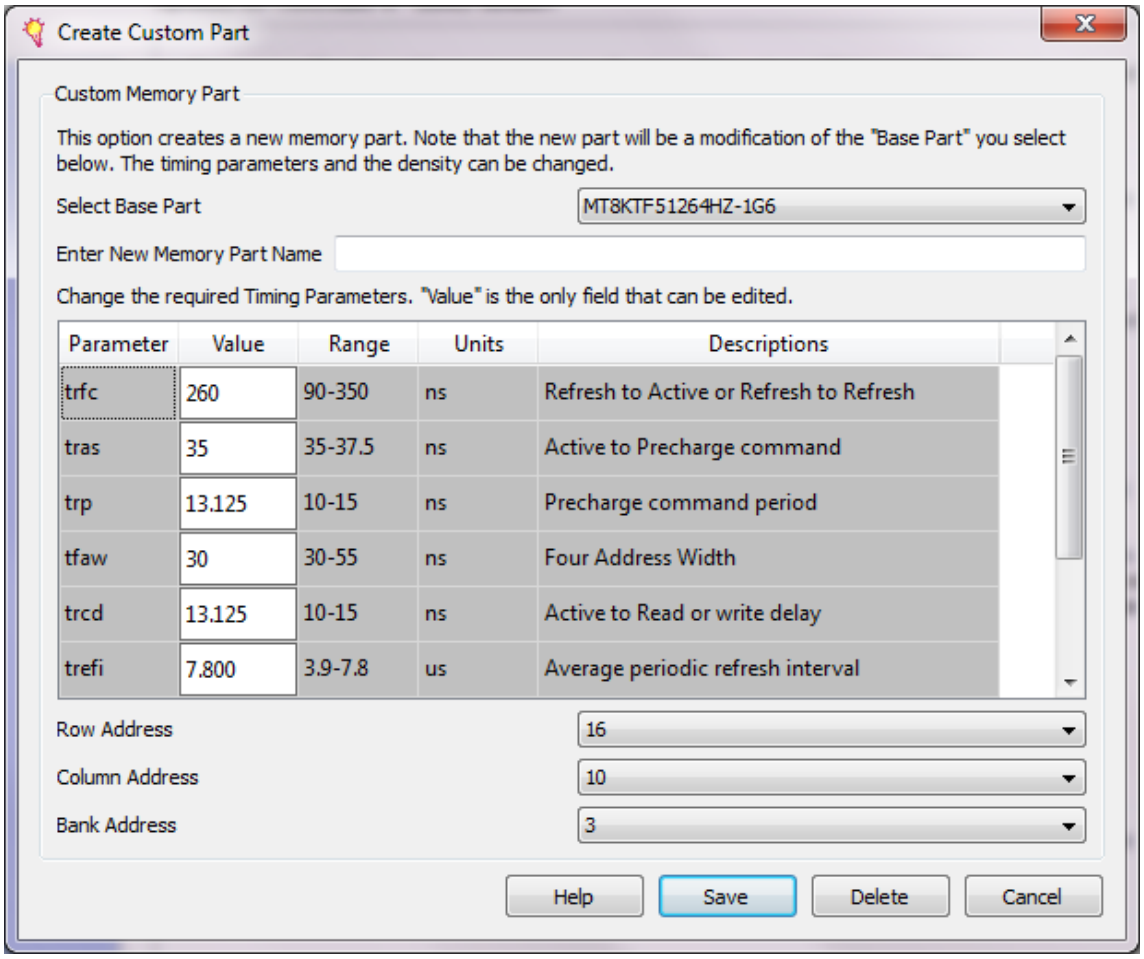


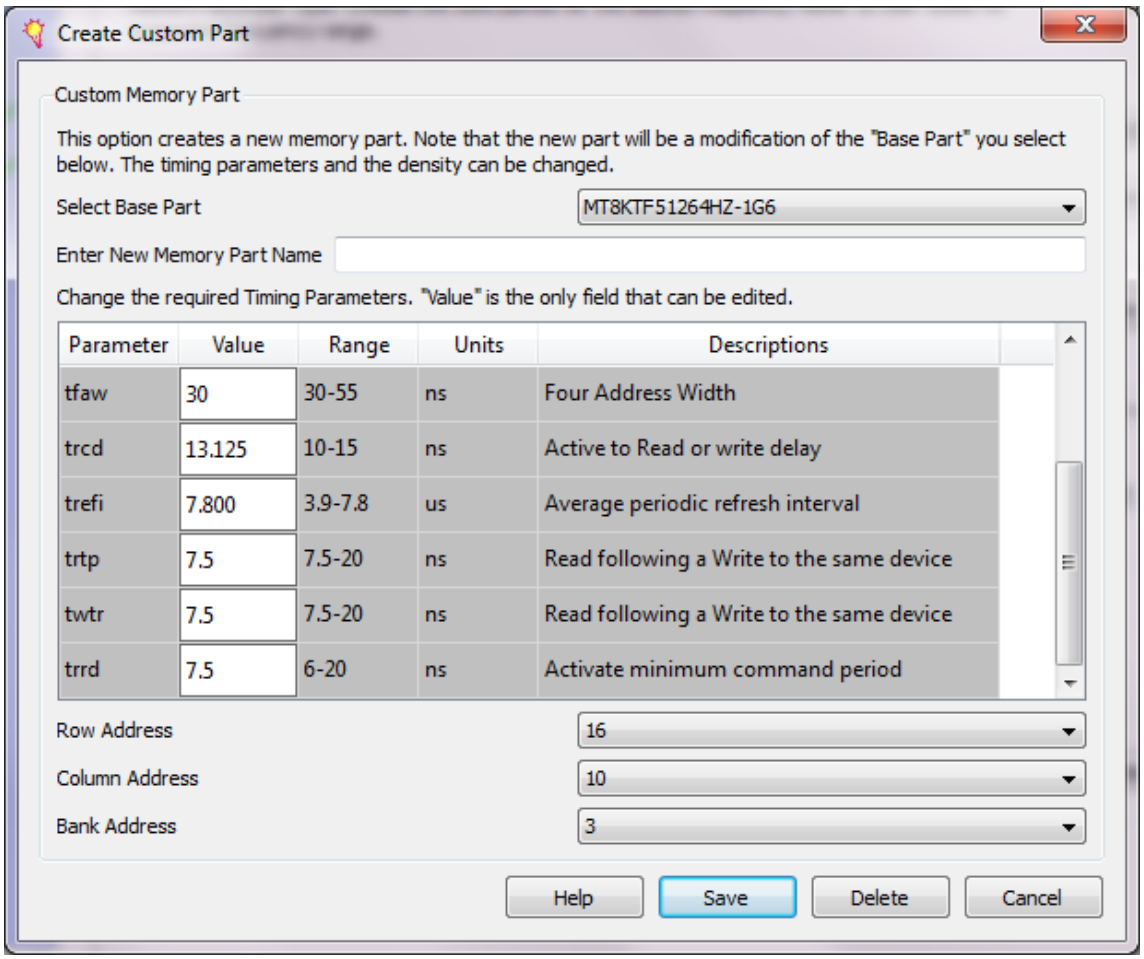

Xilinx Memory Interface Generator
REFERENCE DESIGN
Memory
Interface
Generator
XILINX
MIG Output Options
Create Design
Select this option to generate a new memory controller. Generating a memory controller will create RTL, design constraints (UCF), implementation and simulation files.
Xilinx Reference Boards
Select this option for information on specific designs for Xilinx reference boards.
Verify UCF and Update Design and UCF
Selecting this feature verifies the modified UCF for a design already generated through MIG. It updates the input UCF file to be compatible with the current version of MIG. While updating the UCF it preserves the pin outs of the input UCF. This option will also generate the new design with the Component Name you selected in this page.
Component Name
Please specify the component name for the memory interface. The design directories will be generated under a directory with this name. Three directories will be created "example_design","user_design" and "docs". The user_design will contain the generated memory interface. The example_design adds a simple example application connected to the generated memory interface.
Component Name
crorc_mig_1
Multi-Controller
Up to 8 DDR3 SDRAM controllers or 8 QDRII+ SRAM controllers or a combination of both can be generated. DDR2 and RLDRAM II are not supported for more than 1 controller. The number of controllers that can be accommodated may be limited by the data width and the number of banks utilized.
Number of Controllers
1
Version Info
User Guide
View Data Sheet
< Back
Next>
Cancel

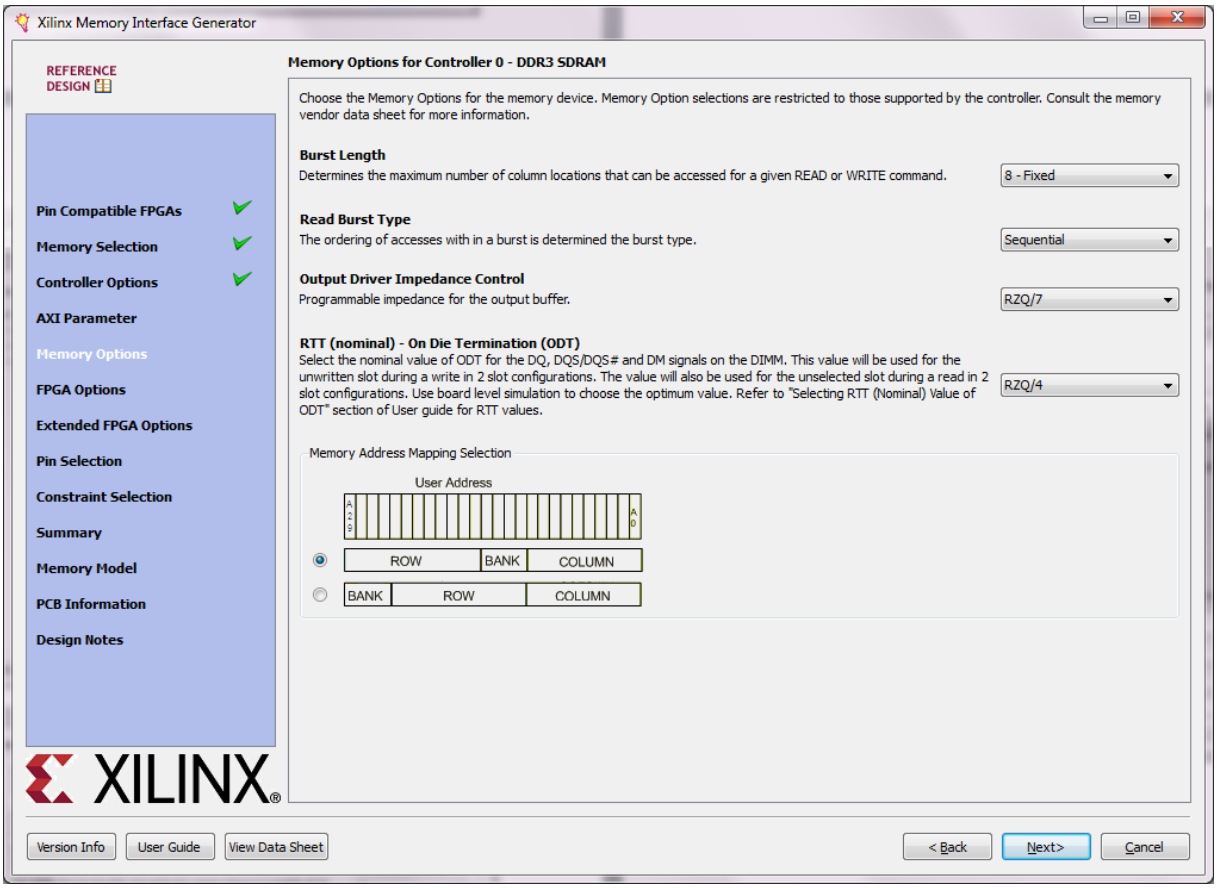

Xilinx Memory Interface Generator
REFERENCE DESIGN
Pin Compatible FPGAs
Memory Selection
Controller Options
AXI Parameter
Memory Options
FPGA Options
Extended FPGA Options
Constraint Selection
Summary
Memory Model
PCB Information
Design Notes
XILINX
Pin Compatible FPGAs
Pin Compatible FPGAs include all devices with the same package and speed grade as the target device. Different FPGA devices with the same package do not have the same bonded pins. By selecting Pin Compatible FPGAs, MIG will only select pins that are common between the target device and all selected devices. Use the default UCF in the par folder for the target part. If you change the target part, use the appropriate UCF in the compatible_ucf folder. If you do not choose a Pin Compatible FPGA now and need to use a different FPGA later, the generated UCF may not work for the new device and a board spin may be required. A device is considered compatible only if the package and speed grade matches to the target part. MIG only ensures that MIG generated pin out is compatible among the selected compatible FPGA devices. Unselected devices will not be considered for compatibility during the pin allocation process.
Blank list indicates that there are no compatible parts exist for the selected target part and this page can be skipped.
Target FPGA
xc6vlx240t-ff1156 -2
Pin Compatible FPGAs
virtex6
lx
xc6vlx130t-ff1156
xc6vlx195t-ff1156
xc6vlx365t-ff1156
sx
xc6vsx475t-ff1156
xc6vsx315t-ff1156
Version Info
User Guide
View Data Sheet
< Back
Next>
Cancel

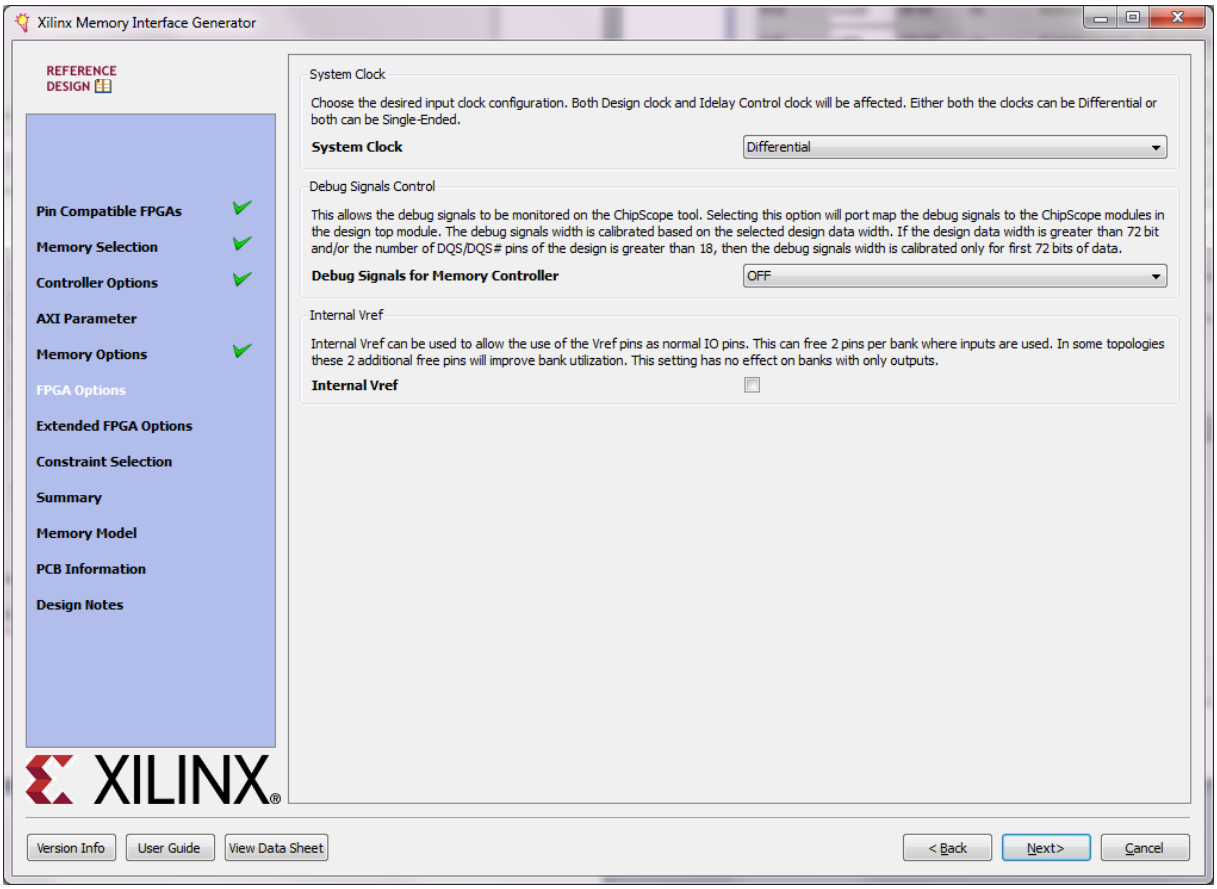

Xilinx Memory Interface Generator
REFERENCE DESIGN
Pin Compatible FPGAs
Memory Selection
Controller Options
AXI Parameter
Memory Options
FPGA Options
Extended FPGA Options
Constraint Selection
Summary
Memory Model
PCB Information
Design Notes
XILINX
Memory Selection
Select the type of memory interface. Please refer to the User Guide for a detailed list of supported controllers for each FPGA family. The list below shows currently available interface(s) for the specific FPGA and speed grade chosen. AXI interface is only supported DDR2 and DDR3 verilog designs.
Select the Controller Type:
DDR3 SDRAM
DDR2 SDRAM
QDRII+ SRAM
RLDRAM II
Version Info
User Guide
View Data Sheet
< Back
Next>
Cancel

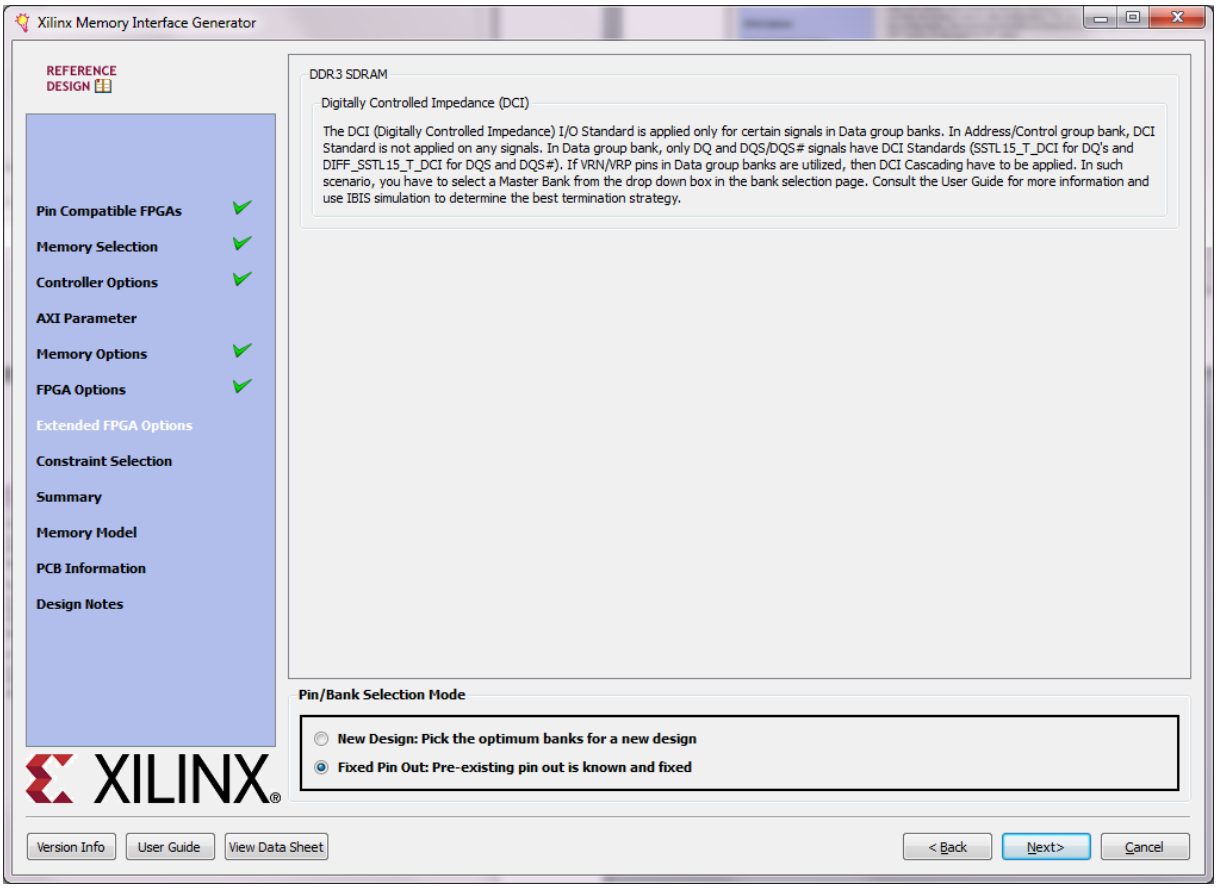

Xilinx Memory Interface Generator
REFERENCE DESIGN
Pin Compatible FPGAs
Memory Selection
Controller Options
AXI Parameter
Memory Options
FPGA Options
Extended FPGA Options
Pin Selection
Constraint Selection
Summary
Memory Model
PCB Information
Design Notes
XILINX
Options for Controller 0 - DDR3 SDRAM
Frequency: The allowed frequency range is a function of the selected FPGA part, FPGA speed grade, and memory controller type. Choose the clock period for the desired frequency. Refer to User Guide for supported frequency range.
2500
ps
400.00 MHz
Memory Type: Select the memory type. Parts marked with a warning symbol are not compatible with the frequency selection above. Based on the FPGA package, DIMMs selection is not allowed due to the unavailability of required number of pins. For RLDRAM II only CIO parts are supported.
SODIMMs
Memory Part: Select the memory part. Parts marked with a warning symbol are not compatible with the frequency selection above. Find an equivalent part or create a part using the "Create Custom Part" button if the part you want is not listed here. The "Create Custom Part" feature is not supported for RLDRAM II.
MT8KTF51264HZ-1G6
Create Custom Part
Data Width: Select the Data Width. Parts marked with a warning symbol are not compatible with the frequency and memory part selected above.
64
ECC: MIG supports ECC for 72 bit and 144 bit data width configurations. To be able to select ECC, you will need to select a data width that has ECC supported.
Disabled
Data Mask: You will be able to enable/disable the generation of Data Mask (DM) pins using this check box. This option can be selectable only if the memory part you have selected has DM pins. Uncheck this box if you would like to not use data masks and save FPGA I/Os that are used for DM signals. ECC designs will not use Data Mask.
ORDERING: Normal mode allows the memory controller to reorder commands to the memory to obtain the highest possible efficiency. Strict mode forces the controller to execute commands in the exact order received.
Normal
Memory Details: 4GB, x16, row:16, col:10, bank:3, unbuffered, data bits per strobe:8, with data mask, single rank
Version Info
User Guide
View Data Sheet
< Back
Next>
Cancel

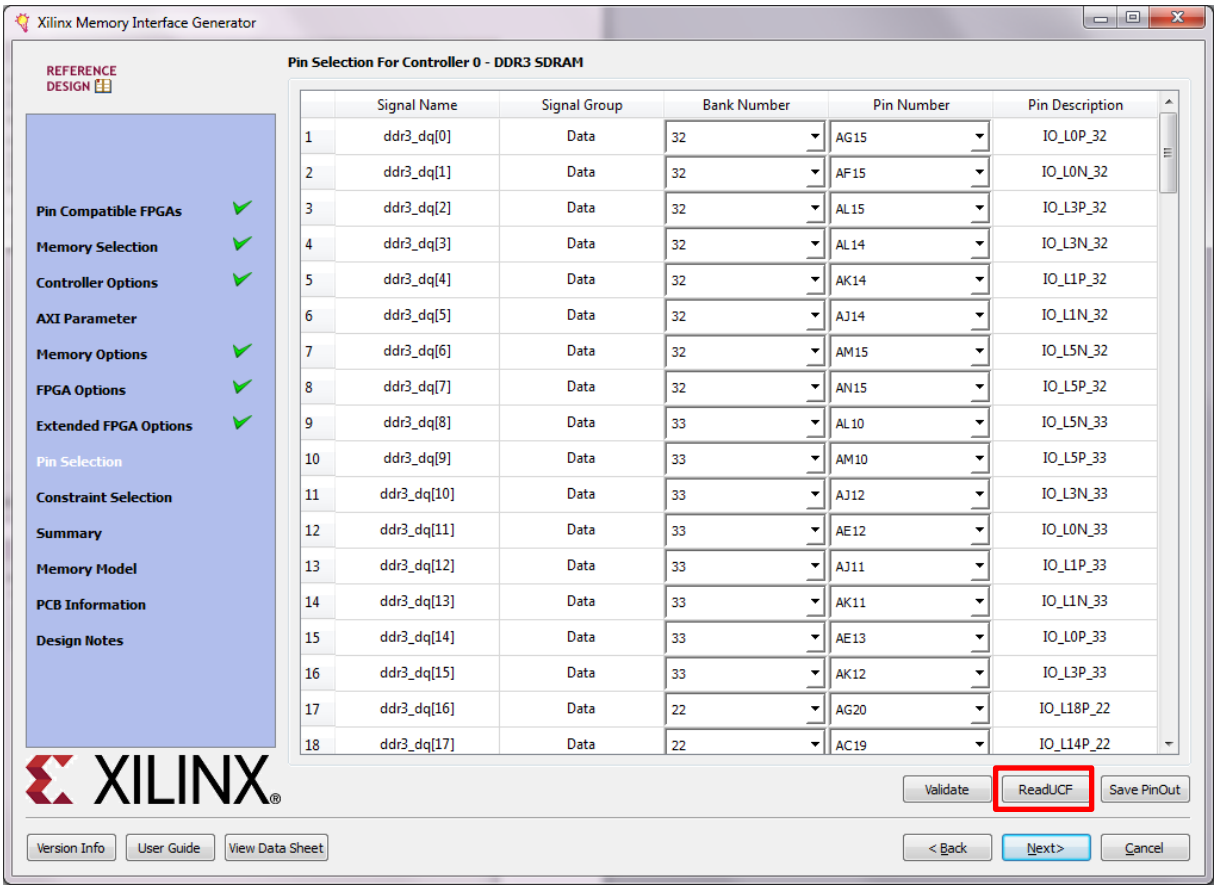

Create Custom Part
Custom Memory Part
This option creates a new memory part. Note that the new part will be a modification of the "Base Part" you select below. The timing parameters and the density can be changed.
Select Base Part
MT8KTF51264HZ-1G6
Enter New Memory Part Name
Change the required Timing Parameters. "Value" is the only field that can be edited.
Parameter
Value
Range
Units
Descriptions
trfc
260
90-350
ns
Refresh to Active or Refresh to Refresh
tras
35
35-37.5
ns
Active to Precharge command
trp
13.125
10-15
ns
Precharge command period
tfaw
30
30-55
ns
Four Address Width
trcd
13.125
10-15
ns
Active to Read or write delay
trefi
7.800
3.9-7.8
us
Average periodic refresh interval
Row Address
16
Column Address
10
Bank Address
3
Help
Save
Delete
Cancel

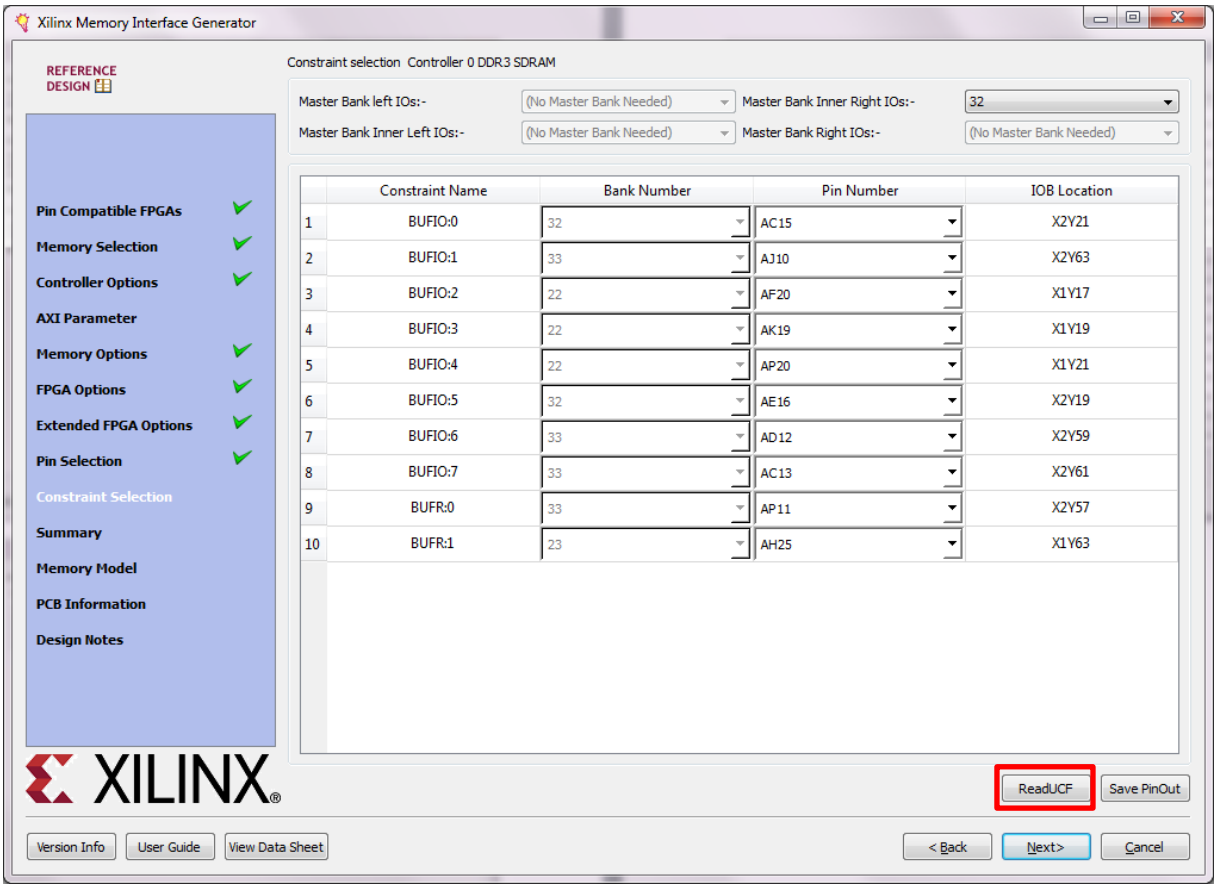

Create Custom Part
Custom Memory Part
This option creates a new memory part. Note that the new part will be a modification of the "Base Part" you select below. The timing parameters and the density can be changed.
Select Base Part
MT8KTF51264HZ-1G6
Enter New Memory Part Name
Change the required Timing Parameters. "Value" is the only field that can be edited.
Parameter
Value
Range
Units
Descriptions
tfaw
30
30-55
ns
Four Address Width
trcd
13.125
10-15
ns
Active to Read or write delay
trefi
7.800
3.9-7.8
us
Average periodic refresh interval
trtp
7.5
7.5-20
ns
Read following a Write to the same device
twtr
7.5
7.5-20
ns
Read following a Write to the same device
trrd
7.5
6-20
ns
Activate minimum command period
Row Address
16
Column Address
10
Bank Address
3
Help
Save
Delete
Cancel


Xilinx Memory Interface Generator
REFERENCE DESIGN
Pin Compatible FPGAs
Memory Selection
Controller Options
AXI Parameter
Memory Options
FPGA Options
Extended FPGA Options
Pin Selection
Constraint Selection
Summary
Memory Model
PCB Information
Design Notes
Memory Options for Controller 0 - DDR3 SDRAM
Choose the Memory Options for the memory device. Memory Option selections are restricted to those supported by the controller. Consult the memory vendor data sheet for more information.
Burst Length
Determines the maximum number of column locations that can be accessed for a given READ or WRITE command.
8 - Fixed
Read Burst Type
The ordering of accesses with in a burst is determined the burst type.
Sequential
Output Driver Impedance Control
Programmable impedance for the output buffer.
RZQ/7
RTT (nominal) - On Die Termination (ODT)
Select the nominal value of ODT for the DQ, DQS/DQS# and DM signals on the DIMM. This value will be used for the unwritten slot during a write in 2 slot configurations. The value will also be used for the unselected slot during a read in 2 slot configurations. Use board level simulation to choose the optimum value. Refer to "Selecting RTT (Nominal) Value of ODT" section of User guide for RTT values.
RZQ/4
Memory Address Mapping Selection
User Address
ROW
BANK
COLUMN
BANK
ROW
COLUMN
XILINX
Version Info
User Guide
View Data Sheet
< Back
Next>
Cancel


Xilinx Memory Interface Generator
REFERENCE DESIGN
Pin Compatible FPGAs
Memory Selection
Controller Options
AXI Parameter
Memory Options
FPGA Options
Extended FPGA Options
Constraint Selection
Summary
Memory Model
PCB Information
Design Notes
System Clock
Choose the desired input clock configuration. Both Design clock and Idelay Control clock will be affected. Either both the clocks can be Differential or both can be Single-Ended.
System Clock
Differential
Debug Signals Control
This allows the debug signals to be monitored on the ChipScope tool. Selecting this option will port map the debug signals to the ChipScope modules in the design top module. The debug signals width is calibrated based on the selected design data width. If the design data width is greater than 72 bit and/or the number of DQS/DQS# pins of the design is greater than 18, then the debug signals width is calibrated only for first 72 bits of data.
Debug Signals for Memory Controller
OFF
Internal Vref
Internal Vref can be used to allow the use of the Vref pins as normal IO pins. This can free 2 pins per bank where inputs are used. In some topologies these 2 additional free pins will improve bank utilization. This setting has no effect on banks with only outputs.
Internal Vref
XILINX
Version Info
User Guide
View Data Sheet
< Back
Next>
Cancel


Xilinx Memory Interface Generator
REFERENCE DESIGN
Pin Compatible FPGAs
Memory Selection
Controller Options
AXI Parameter
Memory Options
FPGA Options
Extended FPGA Options
Constraint Selection
Summary
Memory Model
PCB Information
Design Notes
DDR3 SDRAM
Digitally Controlled Impedance (DCI)
The DCI (Digitally Controlled Impedance) I/O Standard is applied only for certain signals in Data group banks. In Address/Control group bank, DCI Standard is not applied on any signals. In Data group bank, only DQ and DQS/DQS# signals have DCI Standards (SSTL15_T_DCI for DQ's and DIFF_SSTL15_T_DCI for DQS and DQS#). If VRN/VRP pins in Data group banks are utilized, then DCI Cascading have to be applied. In such scenario, you have to select a Master Bank from the drop down box in the bank selection page. Consult the User Guide for more information and use IBIS simulation to determine the best termination strategy.
Pin/Bank Selection Mode
New Design: Pick the optimum banks for a new design
Fixed Pin Out: Pre-existing pin out is known and fixed
XILINX
Version Info
User Guide
View Data Sheet
< Back
Next>
Cancel


Xilinx Memory Interface Generator
REFERENCE DESIGN
Pin Compatible FPGAs
Memory Selection
Controller Options
AXI Parameter
Memory Options
FPGA Options
Extended FPGA Options
Pin Selection
Constraint Selection
Summary
Memory Model
PCB Information
Design Notes
Pin Selection For Controller 0 - DDR3 SDRAM
Signal Name | Signal Group | Bank Number | Pin Number | Pin Description
1 | ddr3_dq[0] | Data | 32 | AG15 | IO_L0P_32
2 | ddr3_dq[1] | Data | 32 | AF15 | IO_L0N_32
3 | ddr3_dq[2] | Data | 32 | AL15 | IO_L3P_32
4 | ddr3_dq[3] | Data | 32 | AL14 | IO_L3N_32
5 | ddr3_dq[4] | Data | 32 | AK14 | IO_L1P_32
6 | ddr3_dq[5] | Data | 32 | AJ14 | IO_L1N_32
7 | ddr3_dq[6] | Data | 32 | AM15 | IO_L5N_32
8 | ddr3_dq[7] | Data | 32 | AN15 | IO_L5P_32
9 | ddr3_dq[8] | Data | 33 | AL10 | IO_L5N_33
10 | ddr3_dq[9] | Data | 33 | AM10 | IO_L5P_33
11 | ddr3_dq[10] | Data | 33 | AJ12 | IO_L3N_33
12 | ddr3_dq[11] | Data | 33 | AE12 | IO_L0N_33
13 | ddr3_dq[12] | Data | 33 | AJ11 | IO_L1P_33
14 | ddr3_dq[13] | Data | 33 | AK11 | IO_L1N_33
15 | ddr3_dq[14] | Data | 33 | AE13 | IO_L0P_33
16 | ddr3_dq[15] | Data | 33 | AK12 | IO_L3P_33
17 | ddr3_dq[16] | Data | 22 | AG20 | IO_L18P_22
18 | ddr3_dq[17] | Data | 22 | AC19 | IO_L14P_22
XILINX
Validate
ReadUCF
Save PinOut
Version Info
User Guide
View Data Sheet
< Back
Next>
Cancel



NOTE: Read ucf in firmware /source/RobinNP_Constraints/CRORC_DDR3Memory_Bank0.ucf or CRORC_DDR3Memory_Bank1.ucf