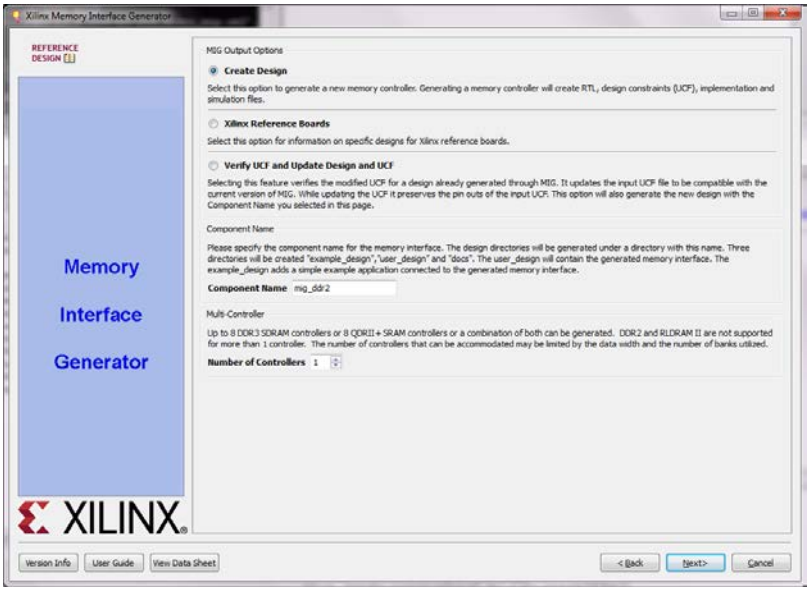
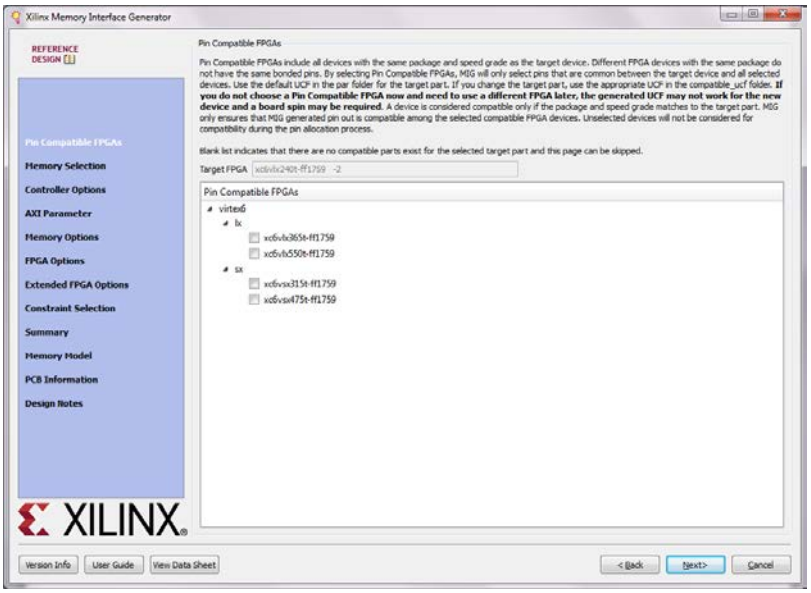
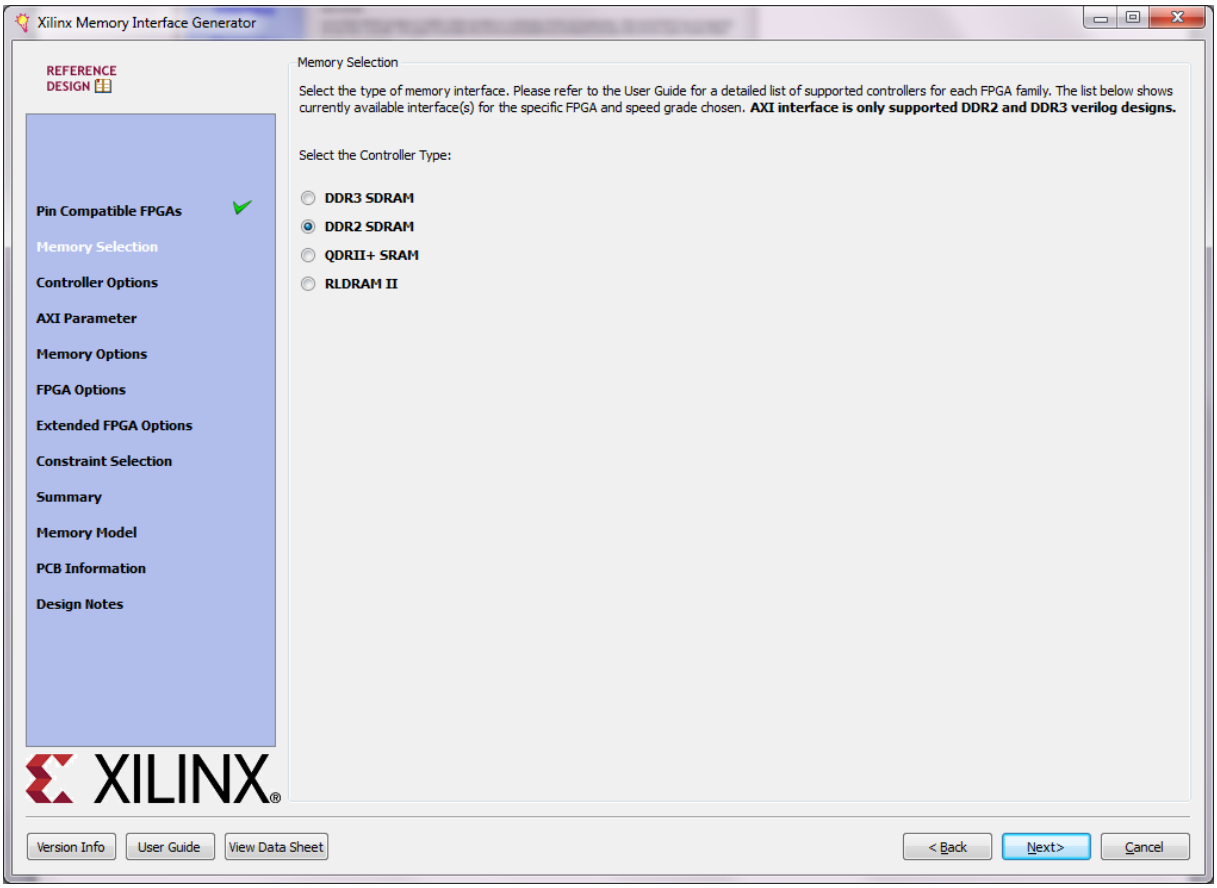
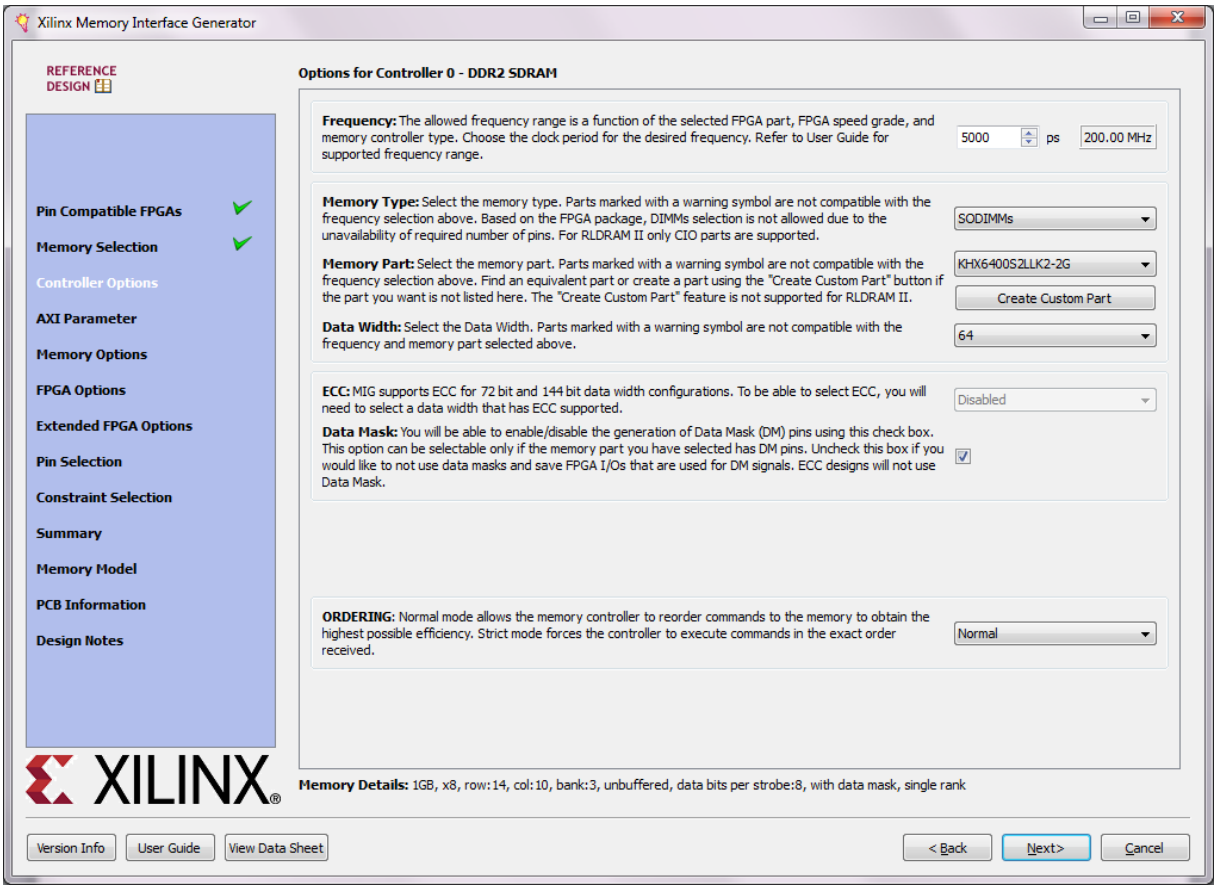
Memory Interface Generator (MIG) notes for the PLDa kit

Core generator (version 13.2) screens:

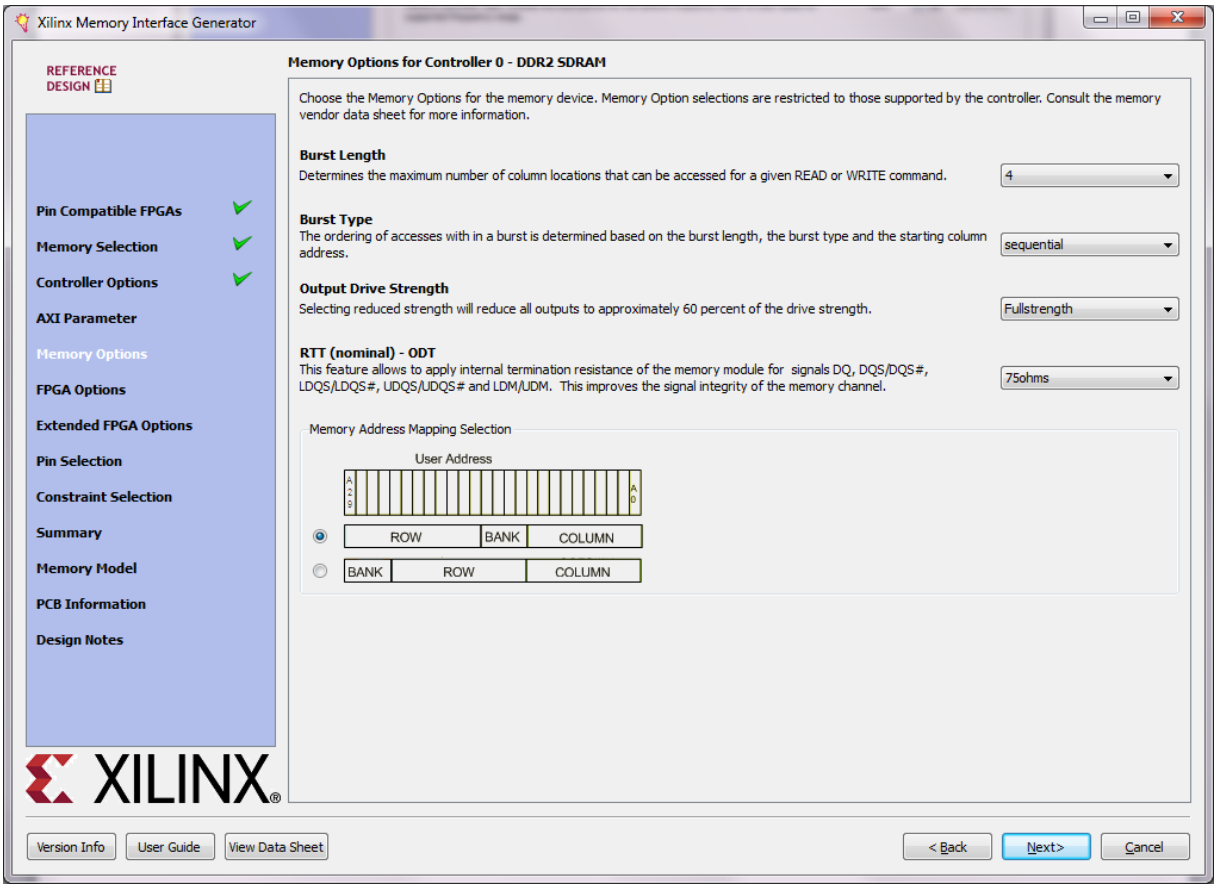


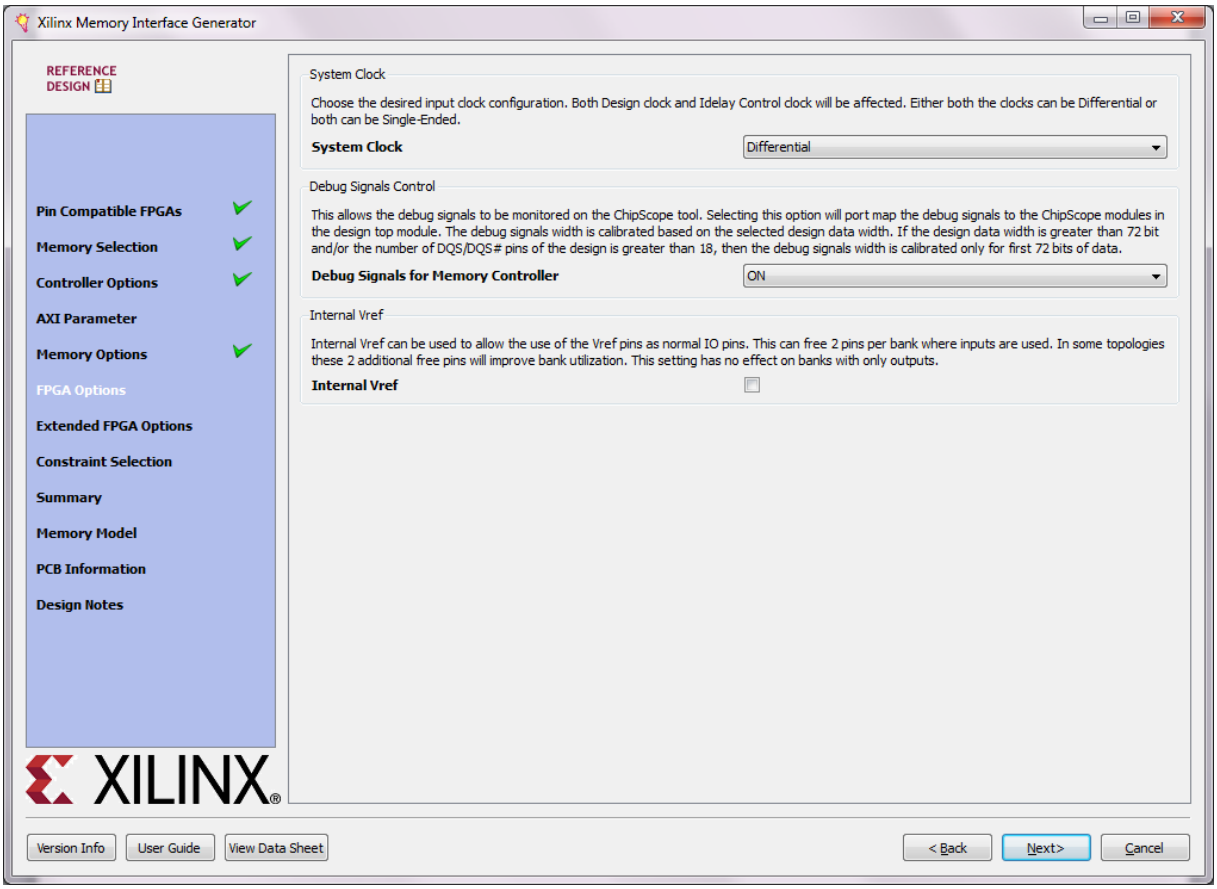


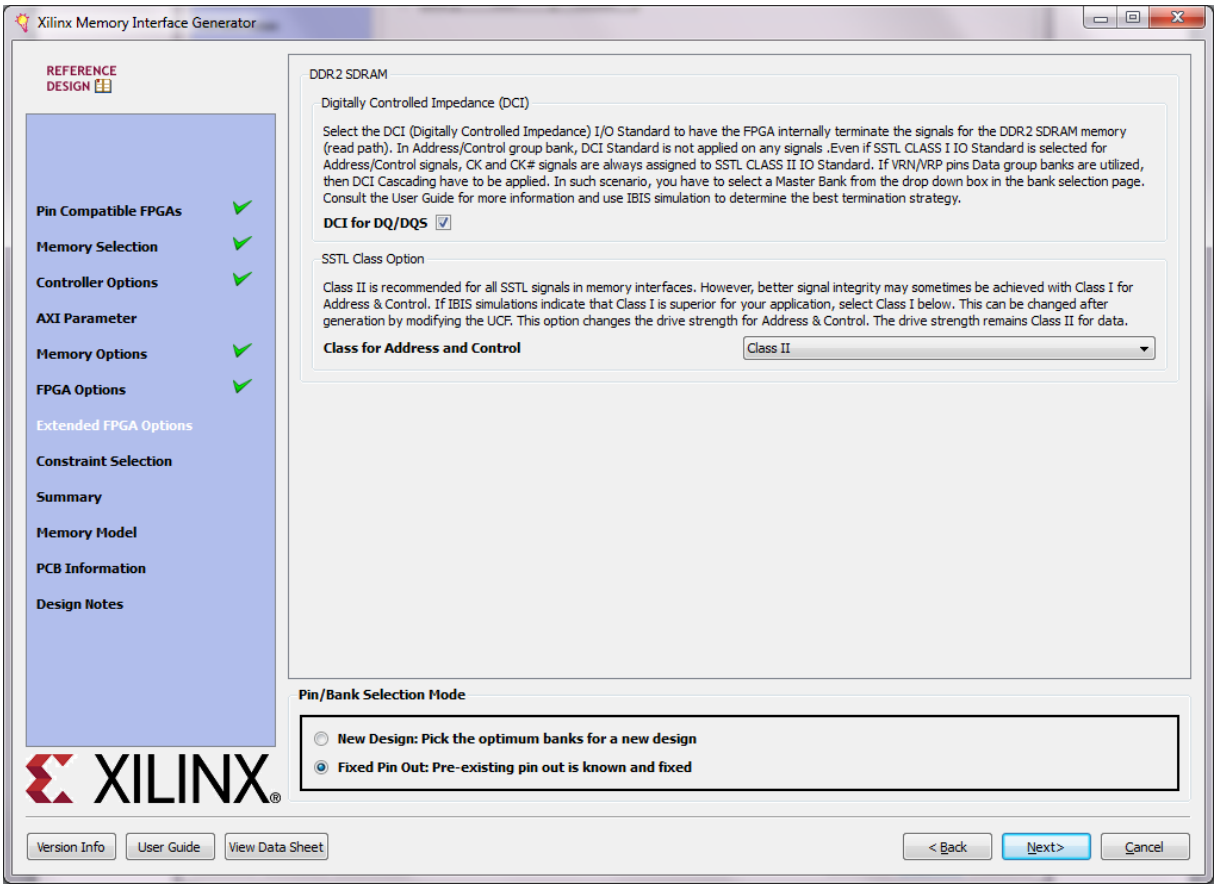


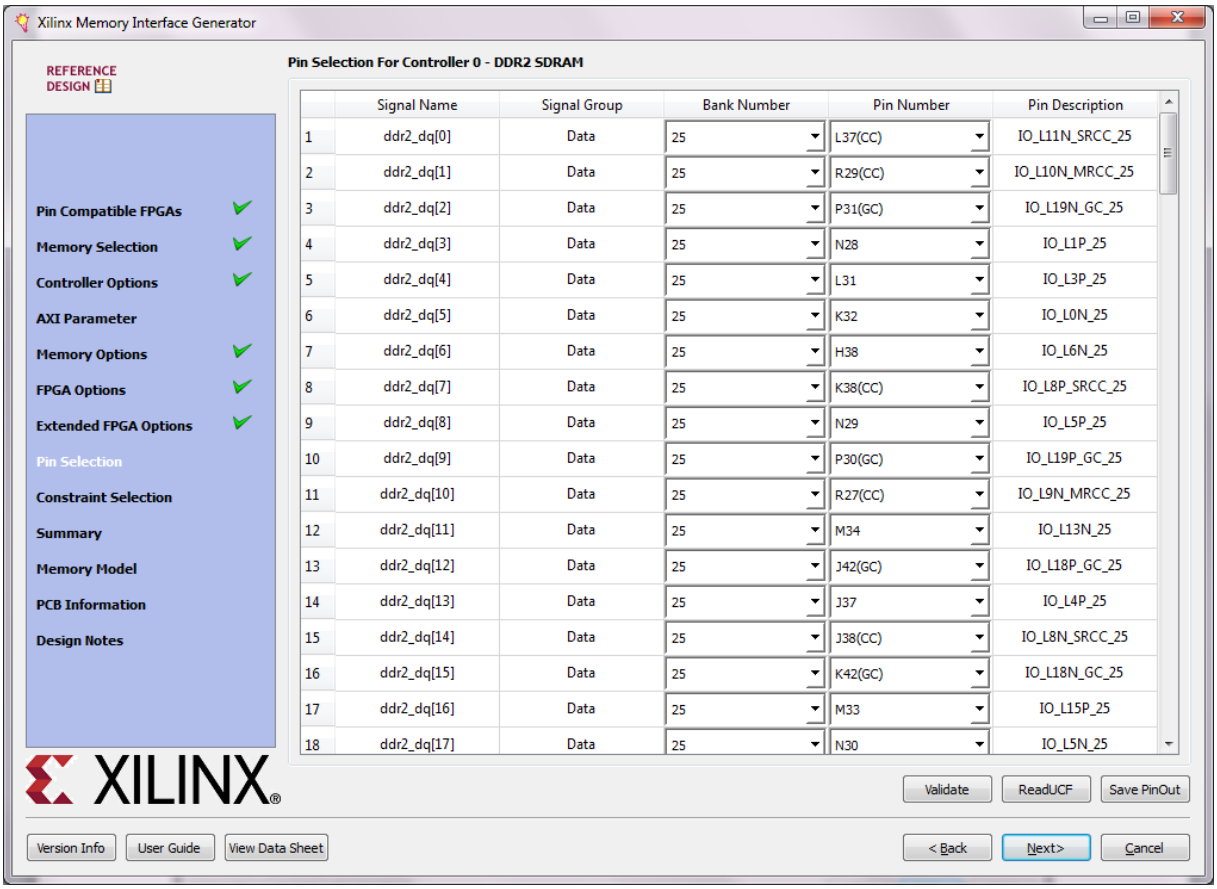


Create custom part for the chosen RAM SODIMM memory bank

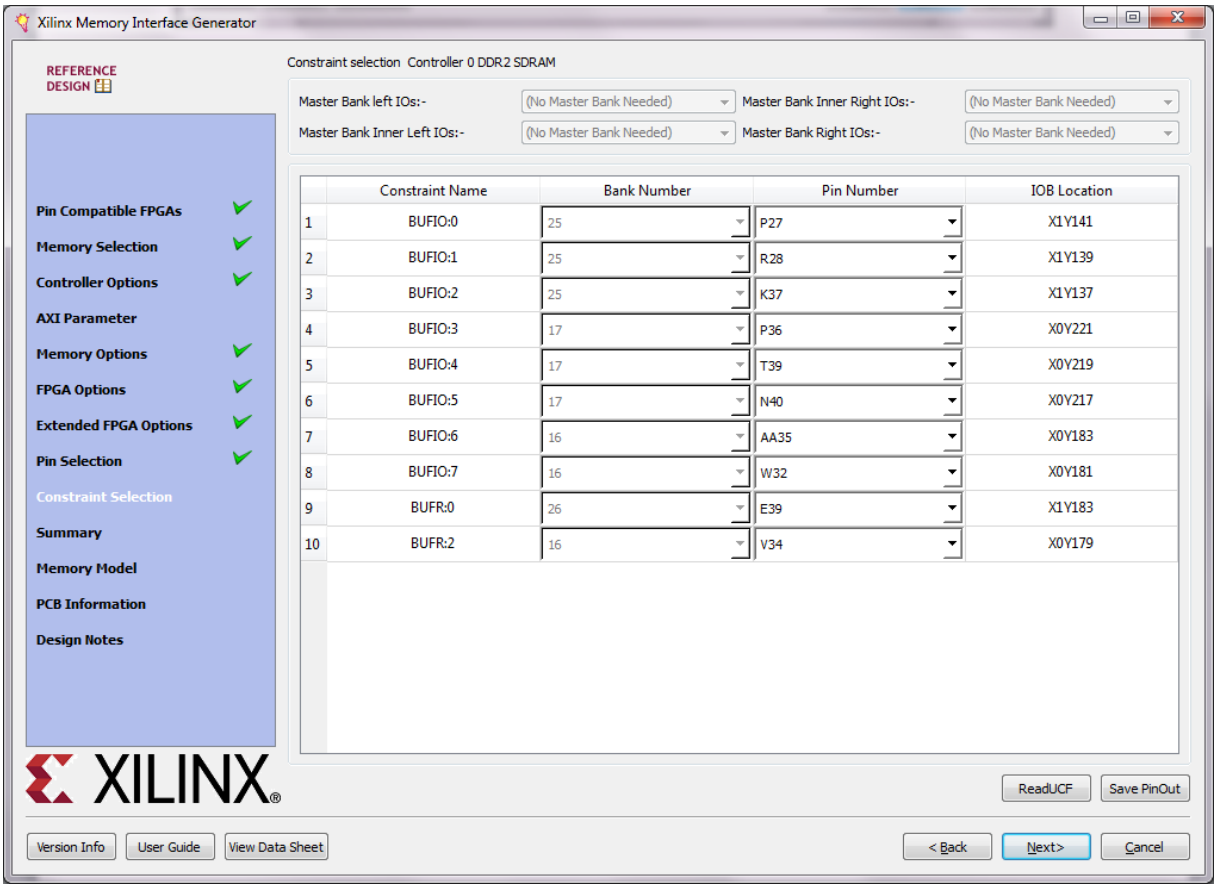

Xilinx Memory Interface Generator
REFERENCE DESIGN
Pin Compatible FPGAs
Memory Selection
Controller Options
AXI Parameter
Memory Options
FPGA Options
Extended FPGA Options
Pin Selection
Constraint Selection
Summary
Memory Model
PCB Information
Design Notes
Memory Options for Controller 0 - DDR2 SDRAM
Choose the Memory Options for the memory device. Memory Option selections are restricted to those supported by the controller. Consult the memory vendor data sheet for more information.
Burst Length
Determines the maximum number of column locations that can be accessed for a given READ or WRITE command.
4
Burst Type
The ordering of accesses with in a burst is determined based on the burst length, the burst type and the starting column address.
sequential
Output Drive Strength
Selecting reduced strength will reduce all outputs to approximately 60 percent of the drive strength.
Fullstrength
RTT (nominal) - ODT
This feature allows to apply internal termination resistance of the memory module for signals DQ, DQS/DQS#, LDQS/LDQS#, UDQS/UDQS# and LDM/UDM. This improves the signal integrity of the memory channel.
75ohms
Memory Address Mapping Selection
User Address
ROW
BANK
COLUMN
BANK
ROW
COLUMN
XILINX
Version Info
User Guide
View Data Sheet
< Back
Next>
Cancel


Xilinx Memory Interface Generator
REFERENCE DESIGN
Pin Compatible FPGAs
Memory Selection
Controller Options
AXI Parameter
Memory Options
FPGA Options
Extended FPGA Options
Constraint Selection
Summary
Memory Model
PCB Information
Design Notes
System Clock
Choose the desired input clock configuration. Both Design clock and Idelay Control clock will be affected. Either both the clocks can be Differential or both can be Single-Ended.
System Clock
Differential
Debug Signals Control
This allows the debug signals to be monitored on the ChipScope tool. Selecting this option will port map the debug signals to the ChipScope modules in the design top module. The debug signals width is calibrated based on the selected design data width. If the design data width is greater than 72 bit and/or the number of DQS/DQS# pins of the design is greater than 18, then the debug signals width is calibrated only for first 72 bits of data.
Debug Signals for Memory Controller
ON
Internal Vref
Internal Vref can be used to allow the use of the Vref pins as normal IO pins. This can free 2 pins per bank where inputs are used. In some topologies these 2 additional free pins will improve bank utilization. This setting has no effect on banks with only outputs.
Internal Vref
XILINX
Version Info
User Guide
View Data Sheet
< Back
Next>
Cancel





Customize your own UCF and import it with “ReadUCF”



Again use the “ReadUCF” to import the IO Buffer constraints

Refeneces for MIG on Virtex-6 devices:

- Virtex-6 FPGA Memory Interface Solutions User Guide (AXI) [ug406].pdf
- Virtex-6 FPGA Memory Interface Solution [ds186].pdf

IMPLEMENTATION Notes [ug406]:

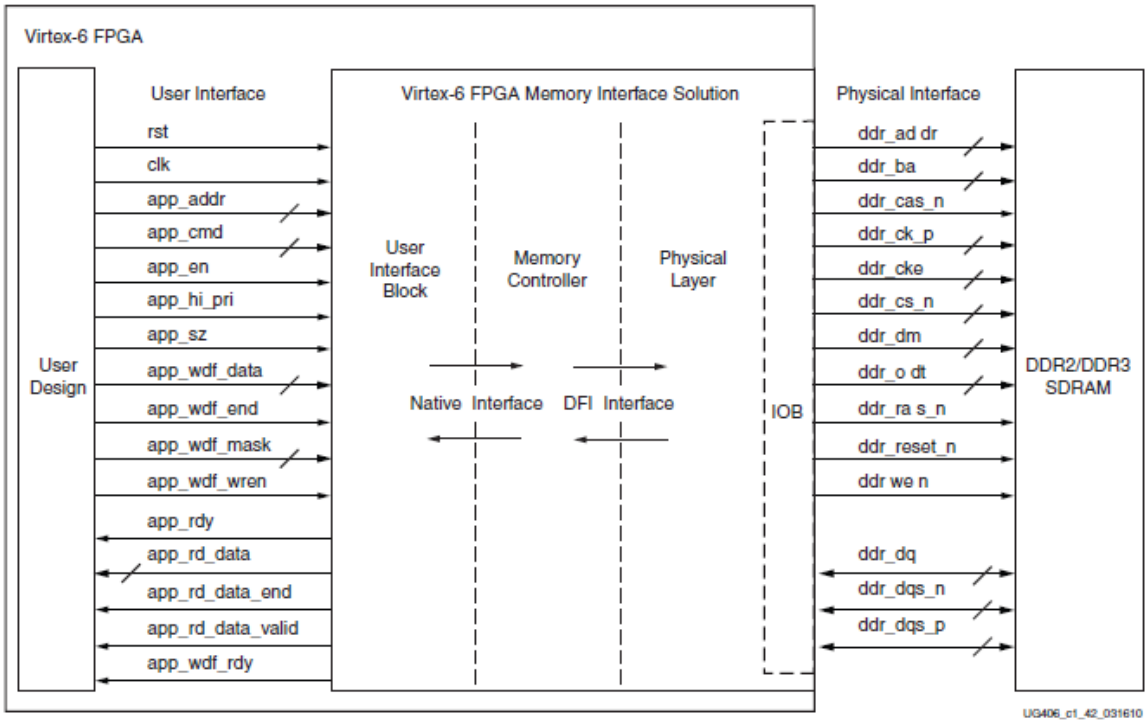


Figure 1-46: **Virtex-6 FPGA Memory Interface Solution**

- **User Interface** design signal description on page 67
- Read about the **Memory Controller** functional description on page 96
- **Physical Interface** signal description on page 112

Useful links :

- Calculate efficiency http://www.xilinx.com/support/answers/36719.htm
- Solution center http://www.xilinx.com/support/answers/34243.htm
- Design assistant http://www.xilinx.com/support/answers/34266.htm
- How do I drive the UI http://www.xilinx.com/support/answers/33698.htm

Forum discussions:

- Addressing the ML605 http://forums.xilinx.com/t5/MIG-Memory-Interface-Generator/Adressing-with-MIG-ML605-and-512-MB/m-p/208347/highlight/true#M2267