231114: Grand Master Source

Issue 2:
After FLASH configure and placement of J7 (i.e. mode[2:0] = “001” Master Serial) the FPGA doesn’t want to configure after powerup. It does configure when pushing S1 “Configure FPGA”.
UG470 Table 2.4 states that R4 must be =< 4K7.
Replace R4 (4K75) with 3K3.