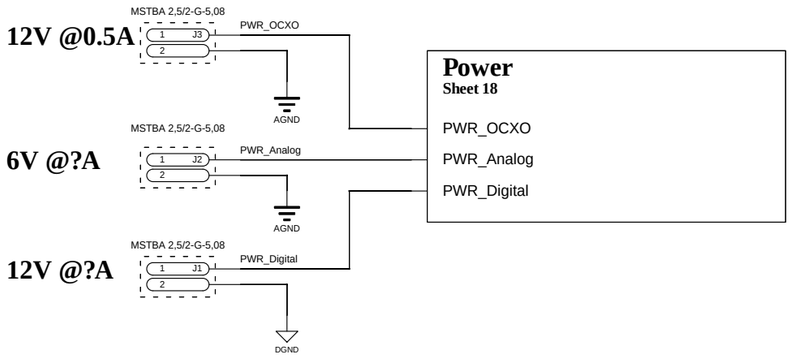


Power
Sheet 18

PWR_OCXO
PWR_Analog
PWR_Digital

WR_Clocks_IO And_Resample
Sheet 16

CLOCK_BUS

Clock_Out_Connectors
Sheet 15

CLOCK_BUS

CLOCK_BUS

FPGA_EEPROM_AND_JTAG
Sheet 8

JTAG
CONFIG
QSPI_BUS

External_SPI_test_Con
Sheet 2

SPI_EXT_TEST

SPI_EXT_TEST

Digital_IO
Sheet 3

LVDS_DAC
LVDS_SPI_PLL

LVDS_DAC
LVDS_SPI_PLL

FPGA_Spartan7
Sheet 4

SPI_EXT_TEST
LVDS_DAC
LVDS_SPI_PLL

JTAG
CONFIG
QSPI_BUS
DAC_LVCMOS
100MHZ_EXT_INT
PLL_SPI_LVCMOS
FPGA_CLK
SWITCH_LED

ISO_SPI_DAC_PLL
Sheet 10

DAC_LVCMOS
100MHZ_EXT_INT
PLL_SPI_LVCMOS
FPGA_CLK

SPI_ISOLATED_DAC
ISO_100MHZ_EXT_INT
Coupled_CLK_IN
SPI_ISOLATED_PLL

OCXO_ASY
Sheet 12

SPI_ISOLATED_DAC
ISO_100MHZ_EXT_INT
Coupled_CLK

100MHz_Out

PLL_ASY
Sheet 14

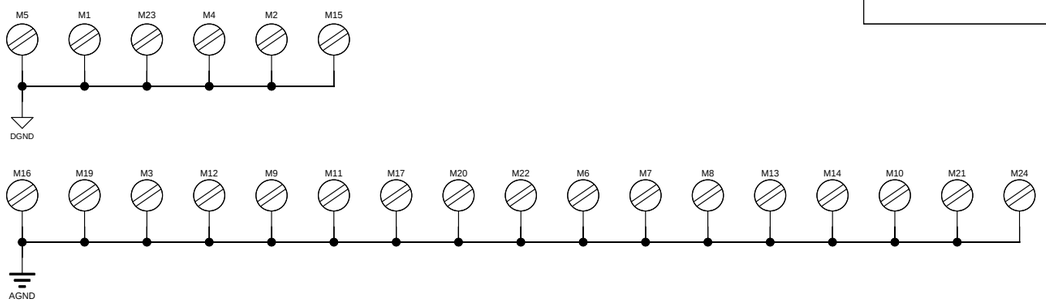
100MHZ_Ref_IN_PLL

CLOCK_BUS

SPI_ISOLATED_PLL

Switch_and_led
Sheet 9

SWITCH_LED



rev.	by	notes

100MHz in the loop v3.0

Project : ET Pathfinder Demonstrator
Sheetname : Schematic1

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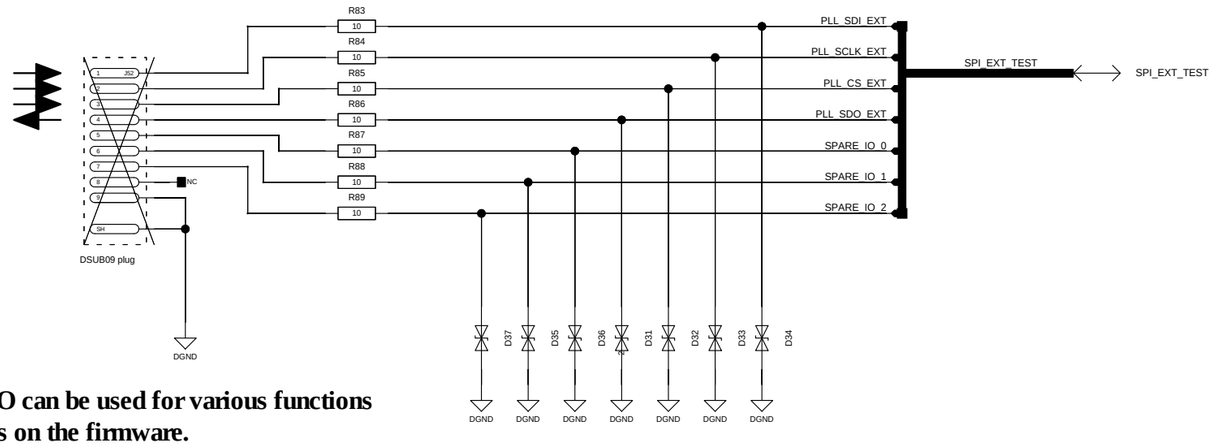
Size 420 x 297mm
Sheet 1 of 21 A3
Date 2023-12-15

Test connector to hookup a microcrontroller.
LVCMOS 3V3! No buffers direct to the FPGA.



Spare IO can be used for various functions depends on the firmware.
Signal direction depends on firmware

rev.	by	notes

100MHz in the loop v3.0

Project : ET Pathfinder Demonstrator
Sheetname : External_SPI_test_Con

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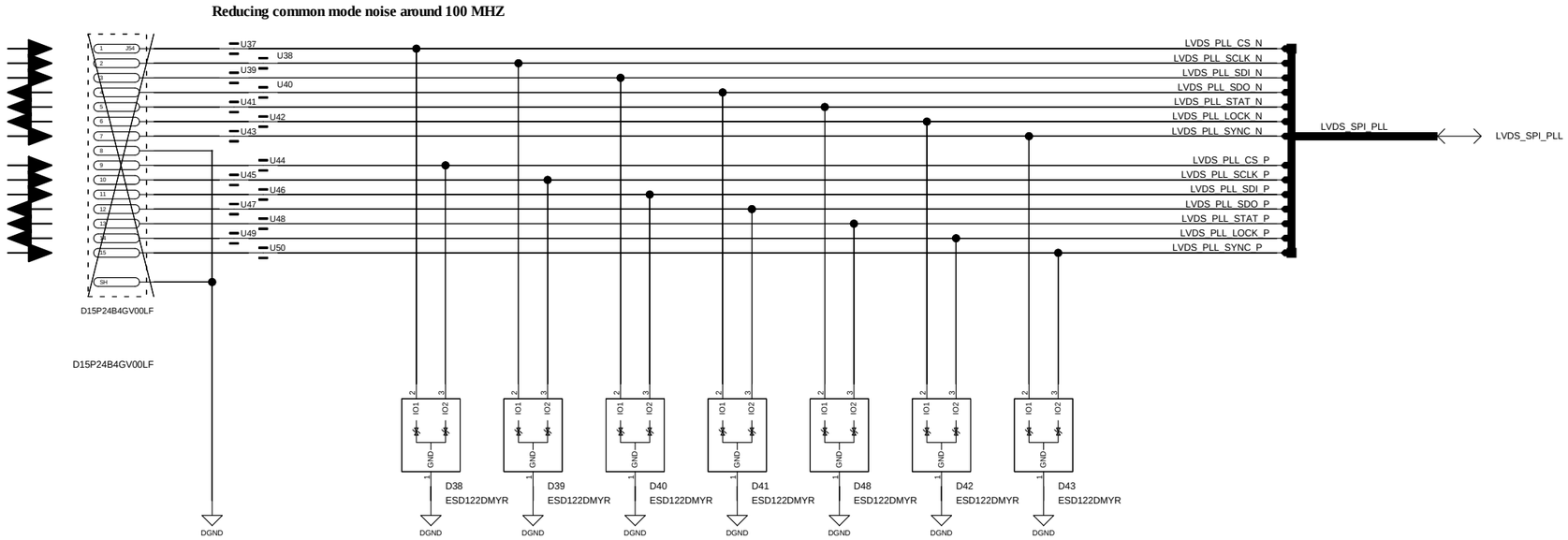
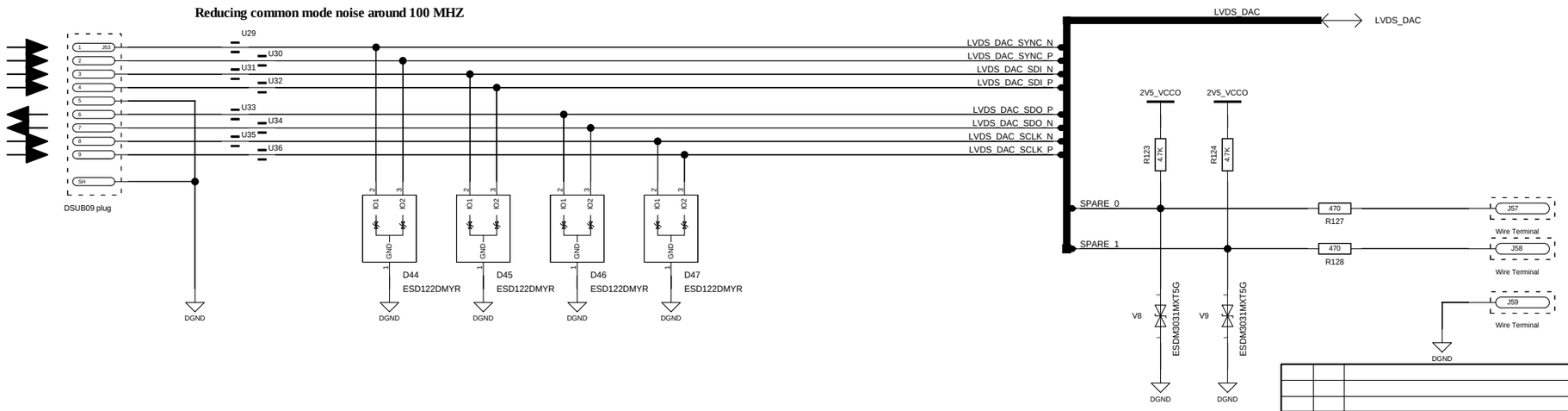
Date 2023-12-15

Connectors PLL Control & DAC



Text on Board =>
LVDS !

From WR. Tune
Reference oscillator.



rev.	by	notes

100MHz in the loop v3.0

Project : ET Pathfinder Demonstrator

Sheetname : Digital_IO

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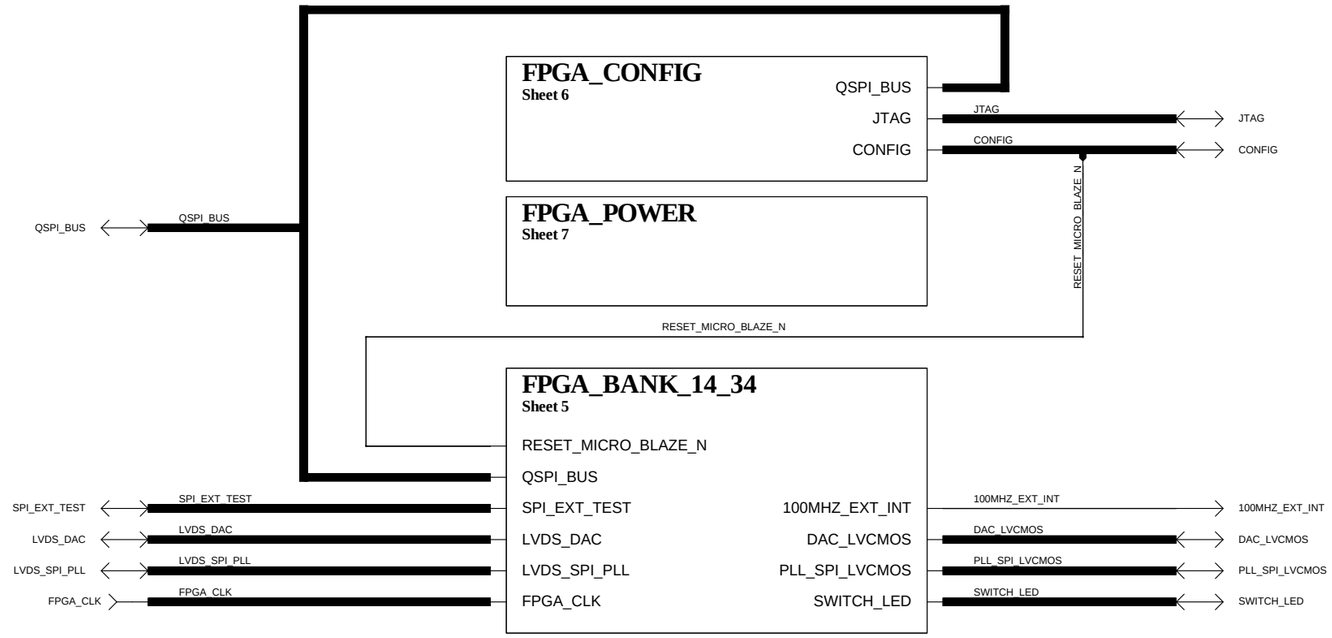

rev.	by	notes

100MHz in the loop v3.0

Project : ET Pathfinder Demonstrator

Sheetname : FPGA_Spartan7

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Sheet 4 of 21 A3

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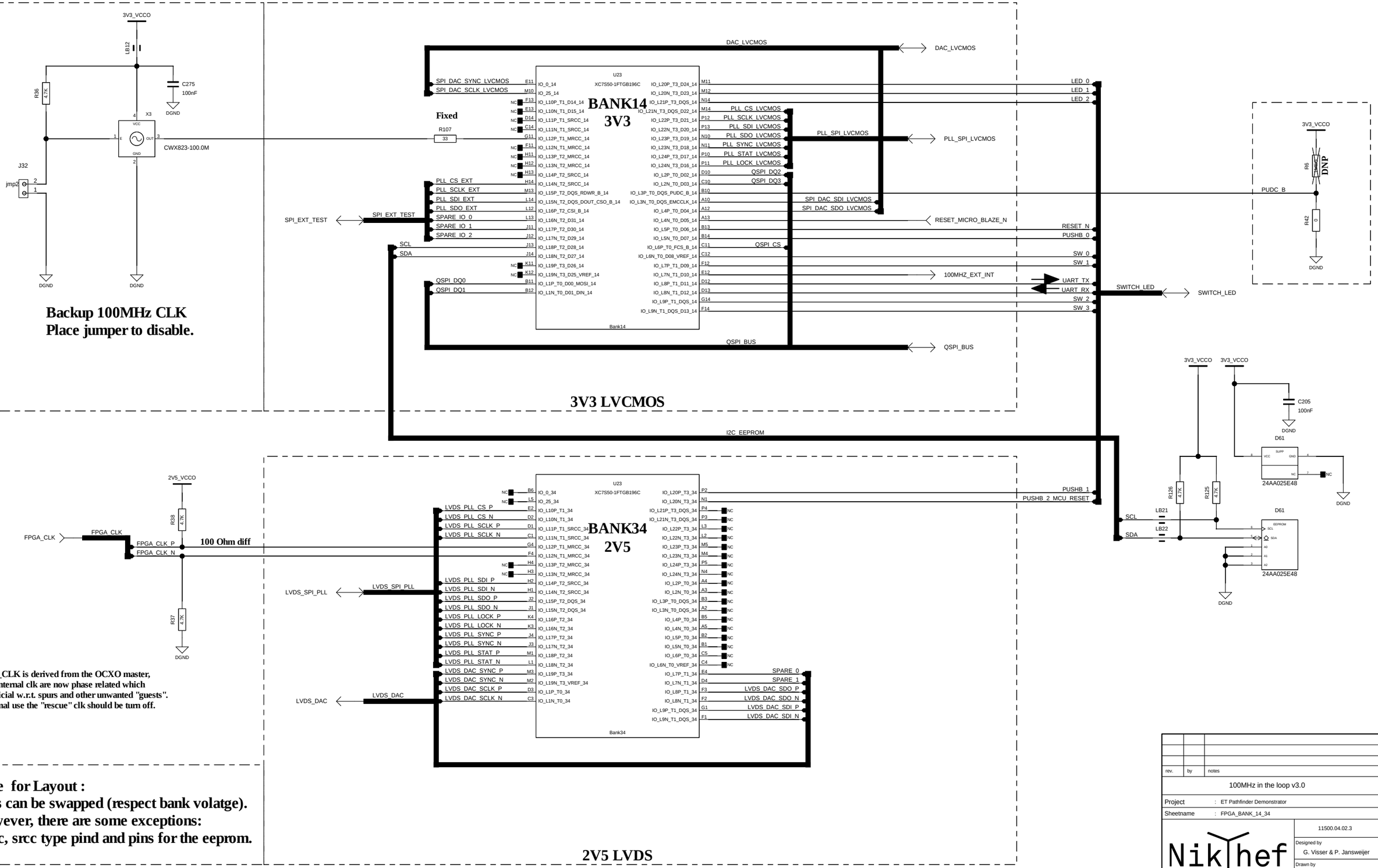

rev.	by	notes

100MHz in the loop v3.0

Project : ET Pathfinder Demonstrator

Sheetname : FPGA_BANK_14_34

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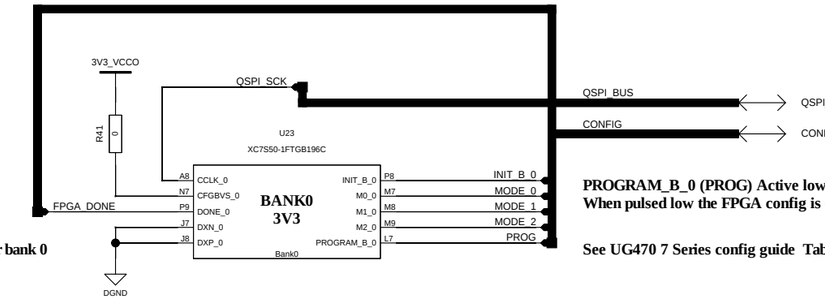
Size 420 x 297mm

Sheet 5 of 21 A3

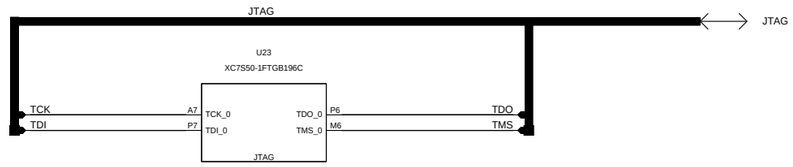
Date 2023-12-15



CFGBVS Pulled to 3V3 this pin selects the voltage IO for bank 0
See UG470 7 Series config guide Table 2-4

PROGRAM_B_0 (PROG) Active low reset.
When pulsed low the FPGA config is cleared and reloaded from FLASH.

See UG470 7 Series config guide Table 4-2



rev.	by	notes

100MHz in the loop v3.0

Project : ET Pathfinder Demonstrator

Sheetname : FPGA_CONFIG

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Sheet 6 of 21 A3

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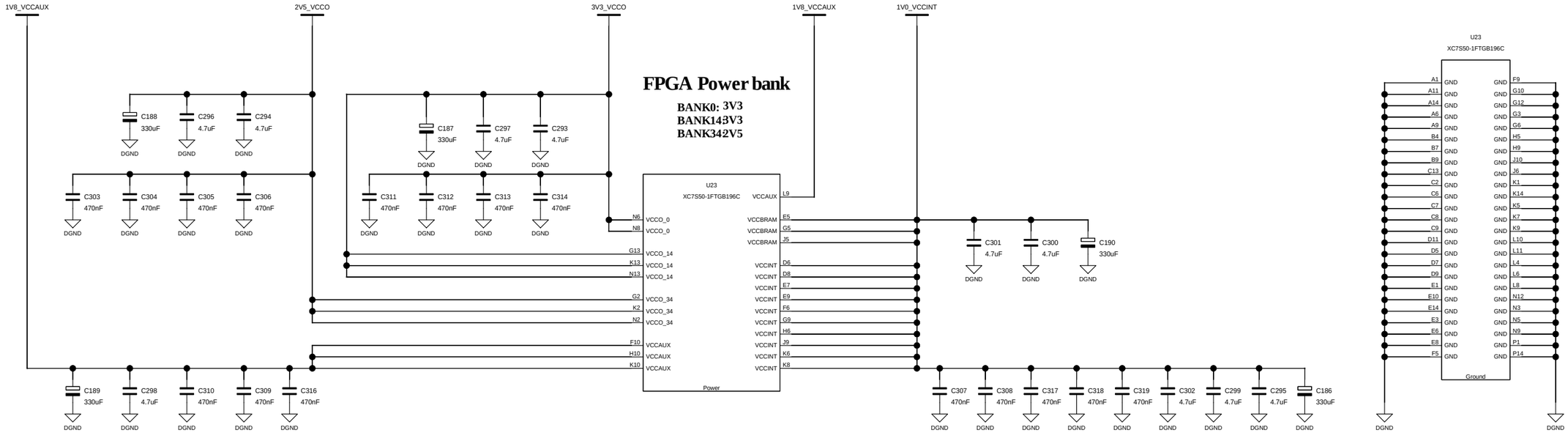
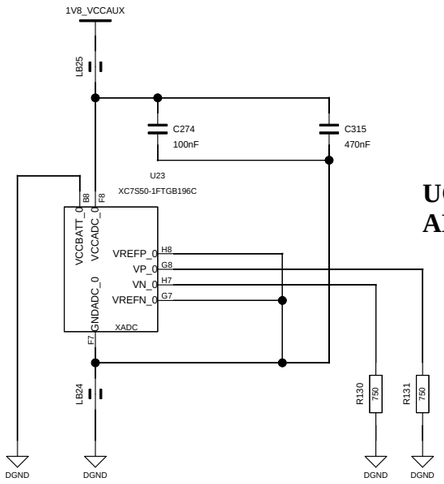


UG483 Table 2-1 (XC7S50 FTGB196):
VCCINT: 1x 100uF, 3x 4.7uF, 5x 0.47uF
VCCBRAM: 1x 100uF, 1x 47uF, 1x 4.7uF, 1x 0.47uF
VCCAUX: 1x 47uF, 1x 4.7uF, 3x 0.47uF
VCCO: 1x 47uF, 2x 4.7uF, 4x 0.47uF

DS189 Table 2 note 9
If battery is not used, connect VCCBATT to either ground or VCCAUX



UG480 Figure 1-2
ADC is not used in this desgin

rev.	by	notes

100MHz in the loop v3.0

Project : ET Pathfinder Demonstrator
Sheetname : FPGA_POWER

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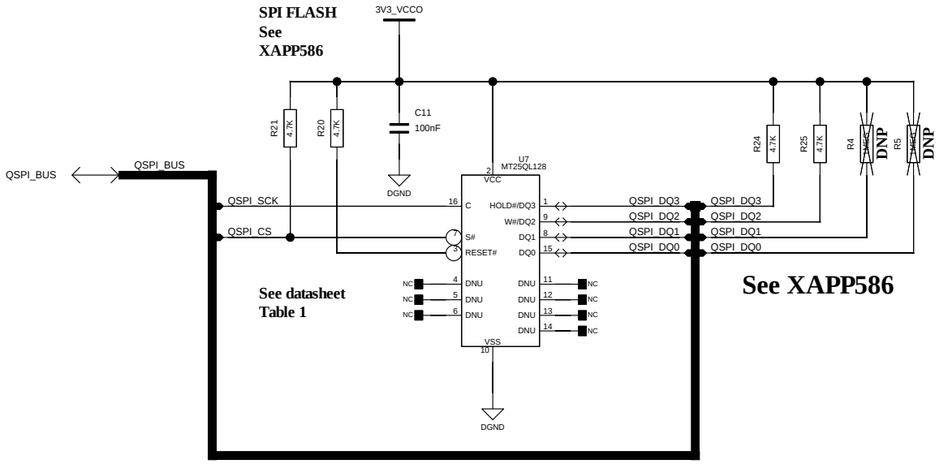
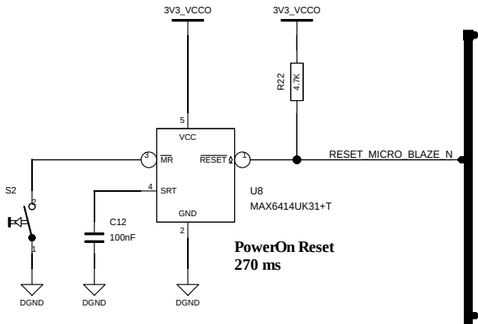
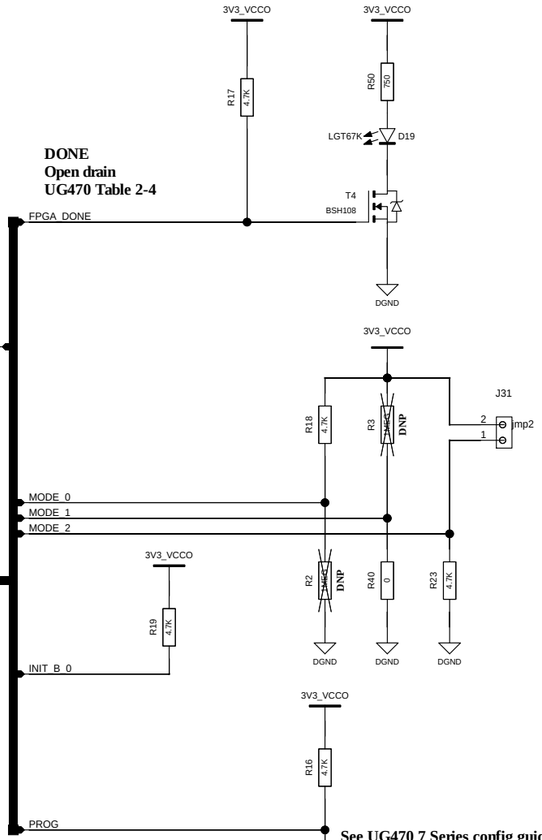
Date 2023-12-15

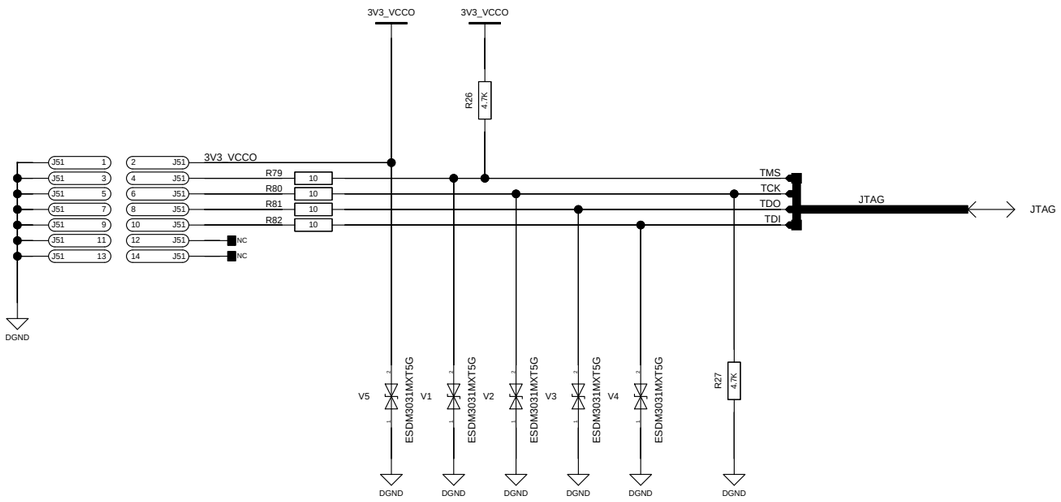






UG470 Table 2-1

Configuration mode	M2	M1	M0	Bush With
Master Serial	0	0	0	x1
Master SPI	0	0	1	x1,x2,x4
Master BPI	0	1	0	x8,x16
	0	1	1	
Master SelectMap	1	0	0	x8,x16
JTAG	1	0	1	x1
Slave SelectMap	1	1	0	x8,x16,x32
Slave Serial	1	1	1	x1



ESD protection

rev.	by	notes

100MHz in the loop v3.0

Project : ET Pathfinder Demonstrator

Sheetname : FPGA_EEPROM_AND_JTAG

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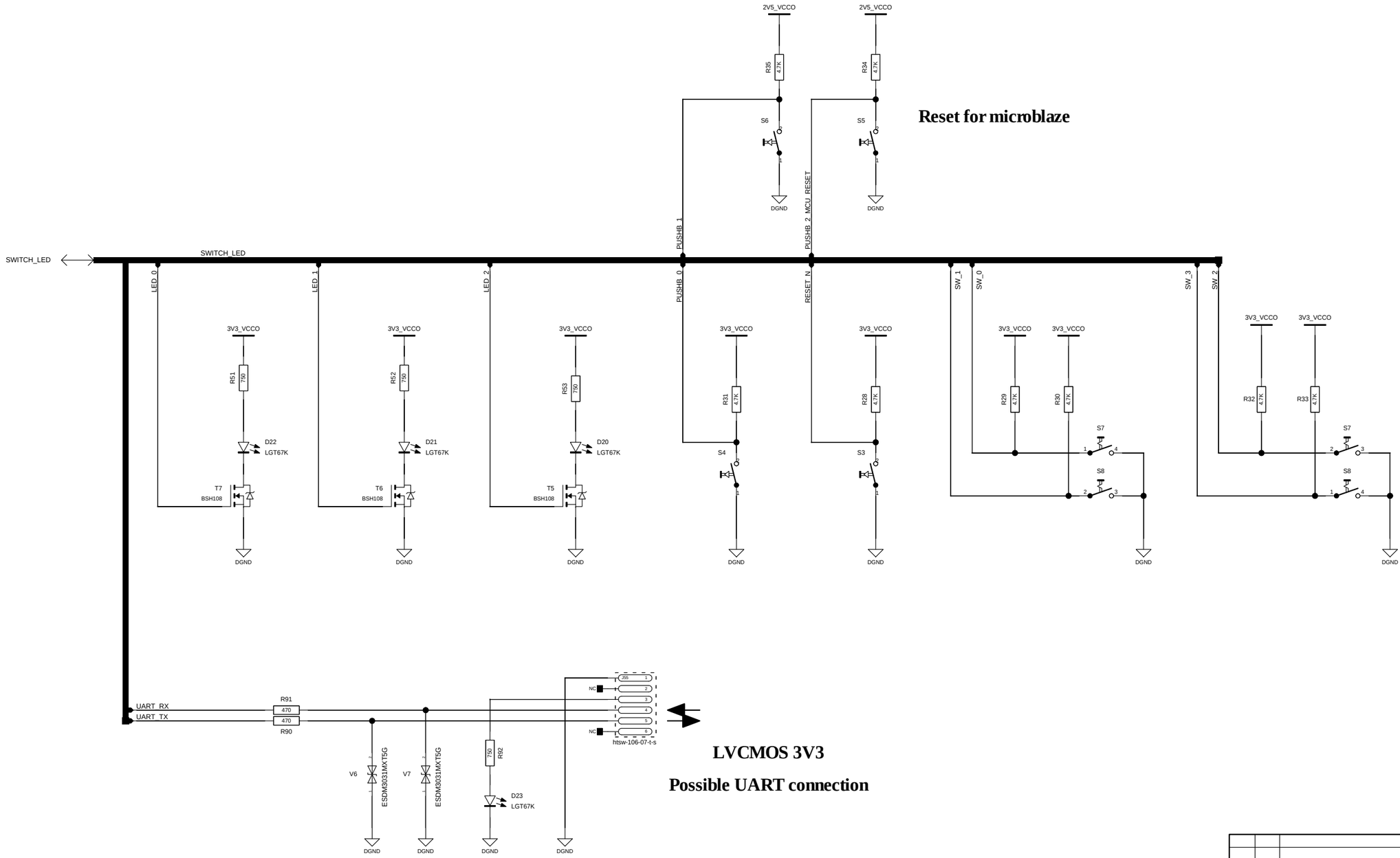

rev.	by	notes

100MHz in the loop v3.0

Project : ET Pathfinder Demonstrator

Sheetname : Switch_and_led

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Sheet: 9 of 21 | A3

Date: 2023-12-15

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Isolation is done to prevent "common mode" noise progation from the fpga to the PLL (conducted)

Digital Domain | **Analog Domain**

PLL_SPI_LVCMOS ⟷ PLL_SPI_LVCMOS

3V3_VCCO, 3V3_PLL

C272 100nF (DGND) — C273 100nF (AGND)

U1 ISO7241

1	VCC1	VCC2	16
3	INA	OUTA	14
4	INB	OUTB	13
5	INC	OUTC	12
6	OUTD	IND	11
7	EN1	EN2	10
2, 8	GND1	GND2	9, 15

PLL_CS_LVCMOS, PLL_SCLK_LVCMOS, PLL_SDI_LVCMOS, PLL_SDO_LVCMOS

PLL_ISO_CS, PLL_ISO_SCLK, PLL_ISO_SDI, PLL_ISO_SDO

PLL_ISO_CS → J39 Wire Terminal **PLL_ISO_CS**
PLL_ISO_SCLK → J40 Wire Terminal **PLL_ISO_SCLK**
PLL_ISO_SDI → J41 Wire Terminal **PLL_ISO_SDI**
PLL_ISO_SDO → J42 Wire Terminal **PLL_ISO_SDO**
PLL_ISO_SYNC → J43 Wire Terminal **PLL_ISO_SYNC**
J44 Wire Terminal **AGND**

Text onboard

SPI_ISOLATED_PLL ⟷ SPI_ISOLATED_PLL

3V3_VCCO, 3V3_PLL

C270 100nF (DGND) — C271 100nF (AGND)

U2 ISO7241

16	VCC2	VCC1	1
14	OUTA	INA	3
13	OUTB	INB	4
NC	OUTC	INC	5
11	IND	OUTD	6
10	EN2	EN1	7
15, 9	GND2	GND1	8, 2

PLL_STAT_LVCMOS, PLL_LOCK_LVCMOS, PLL_SYNC_LVCMOS

PLL_ISO_STAT, PLL_ISO_LOCK, PLL_ISO_SYNC

R46 47K (AGND)

5V_DAC

LB34

C324 100nF (AGND) — C323 100nF (AGND)

R155 1K — R154 100

C325 1.5nF (AGND) — U52 SN74LVC1G04 — C326 1.5nF (AGND) — U53 SN74LVC1G00

Digital Latency delay (1.5 us)

LDAC pulse width (150 ns)

20 Bit DAC MAX5719A needs a signal (LDAC_n) to load the SPI shifted bits into the DAC section. This signal is derived from the rising edge of SYNC_n.

3V3_VCCO

C268 100nF (DGND) — C269 100nF (AGND)

U3 ISO7241

1	VCC1	VCC2	16
3	INA	OUTA	14
4	INB	OUTB	13
5	INC	OUTC	12
6	OUTD	IND	11
7	EN1	EN2	10
2, 8	GND1	GND2	9, 15

DAC_LVCMOS ⟷ DAC_LVCMOS

SPI_DAC_SYNC_LVCMOS, SPI_DAC_SCLK_LVCMOS, SPI_DAC_SDI_LVCMOS, SPI_DAC_SDO_LVCMOS

SPI_ISO_DAC_SYNC, SPI_ISO_DAC_SCLK, SPI_ISO_DAC_SDI, SPI_ISO_DAC_SDO

R45 47K (AGND)

SPI_ISO_DAC_LDAC → J67 Wire Terminal **SPI_ISO_DAC_LDAC**
SPI_ISO_DAC_SYNC → J34 Wire Terminal **SPI_ISO_DAC_SYNC**
SPI_ISO_DAC_SCLK → J35 Wire Terminal **SPI_ISO_DAC_SCLK**
SPI_ISO_DAC_SDI → J37 Wire Terminal **SPI_ISO_DAC_SDI**
SPI_ISO_DAC_SDO → J36 Wire Terminal **SPI_ISO_DAC_SDO**
J38 Wire Terminal **AGND**

Text onboard

SPI_ISOLATED_DAC ⟷ SPI_ISOLATED_DAC

CLK_SHAPER
Sheet 11

FPGA_CLK ⟷ FPGA_CLK — FPGA_CLK — Coupled_CLK_IN — Coupled_CLK_IN ⟷ Coupled_CLK_IN

100MHZ_EXT_INT = LVCMOS 3V3
Drive"1" to enable internal OCXO

100MHZ_EXT_INT ⟷ 100MHZ_EXT_INT — R47 1K — U4 CPC1018N — ISO_100MHZ_EXT_INT ⟷ ISO_100MHZ_EXT_INT

rev.	by	notes
		100MHz in the loop v3.0

Project : ET Pathfinder Demonstrator
Sheetname : ISO_SPI_DAC_PLL

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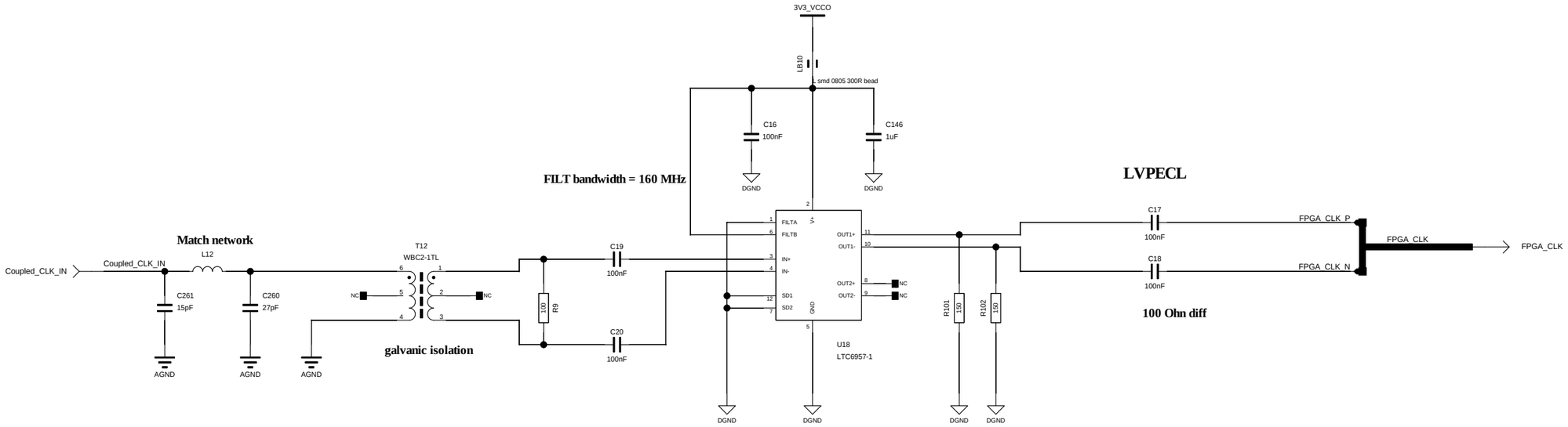
Size 420 x 297mm
Sheet 10 of 21 A3
Date 2023-12-15



FPGA clk Shaphing and isolating

rev.	by	notes

100MHz in the loop v3.0

Project : ET Pathfinder Demonstrator

Sheetname : CLK_SHAPER

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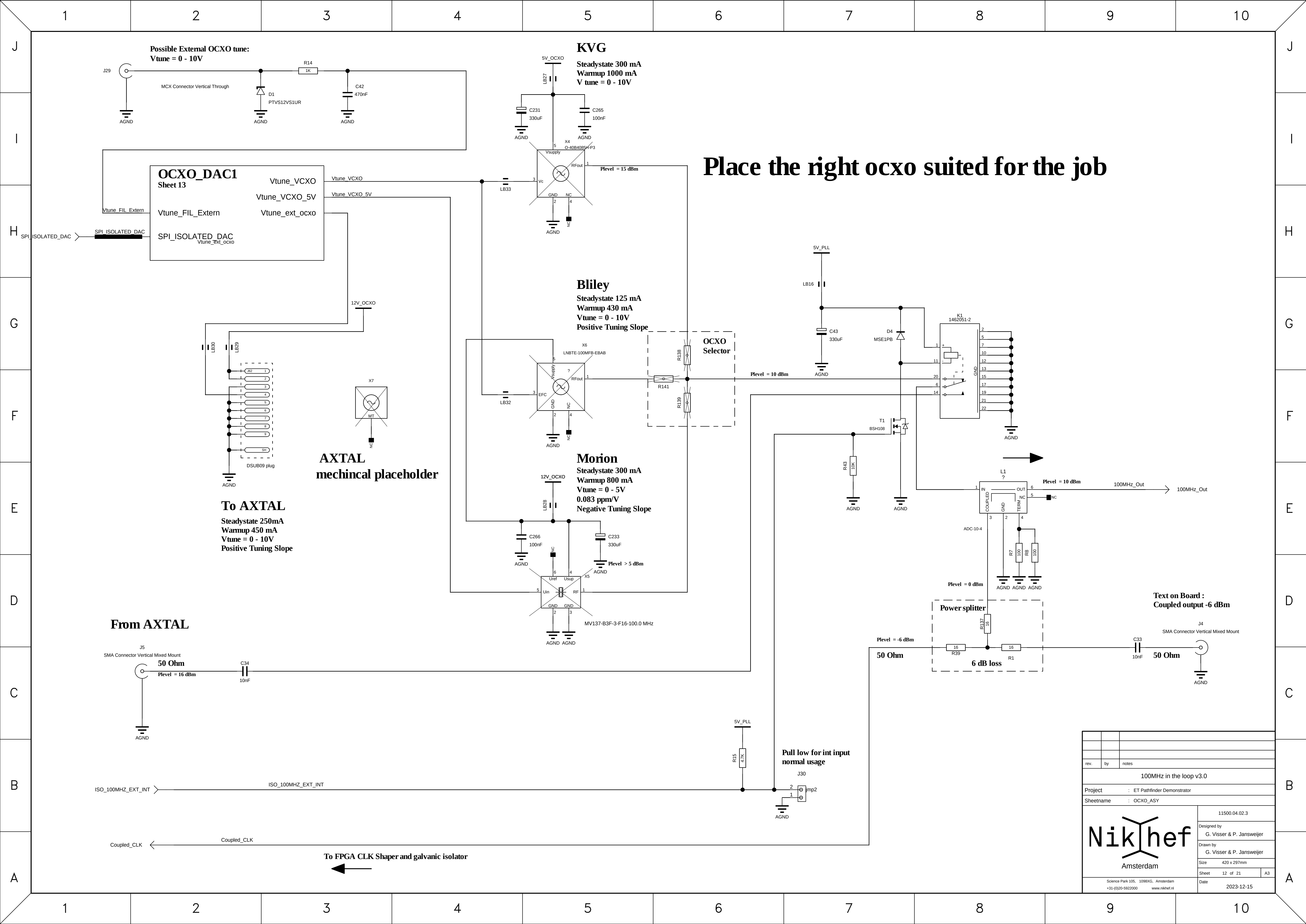
Size: 420 x 297mm

Sheet: 11 of 21 A3

Date: 2023-12-15



Possible External OCXO tune:
Vtune = 0 - 10V
J29
MCX Connector Vertical Through
D1
PTVS12VS1UR
R14
1K
C42
470nF
AGND
KVG
Steadystate 300 mA
Warmup 1000 mA
V tune = 0 - 10V
5V_OCXO
LB27
C231
330uF
C265
100nF
X4
O-40B4085H-P3
Vsupply
RFout
Vc
GND
NC
Plevel = 15 dBm
LB33
Place the right ocxo suited for the job
OCXO_DAC1
Sheet 13
Vtune_VCXO
Vtune_VCXO_5V
Vtune_ext_ocxo
Vtune_FIL_Extern
SPI_ISOLATED_DAC
12V_OCXO
LB30
LB29
DSUB09 plug
X7
MT
AXTAL
mechincal placeholder
Bliley
Steadystate 125 mA
Warmup 430 mA
Vtune = 0 - 10V
Positive Tuning Slope
X6
LNBTE-100MFB-EBAB
EFC
LB32
OCXO
Selector
R138
R139
R141
Plevel = 10 dBm
5V_PLL
LB16
C43
330uF
D4
MSE1PB
K1
1462051-2
T1
BSH108
R43
10K
Morion
Steadystate 300 mA
Warmup 800 mA
Vtune = 0 - 5V
0.083 ppm/V
Negative Tuning Slope
LB28
C266
100nF
C233
330uF
Plevel > 5 dBm
X5
Uref
Usup
Uin
RF
MV137-B3F-3-F16-100.0 MHz
To AXTAL
Steadystate 250mA
Warmup 450 mA
Vtune = 0 - 10V
Positive Tuning Slope
L1
IN
OUT
COUPLED
TERM
ADC-10-4
Plevel = 10 dBm
100MHz_Out
R7
R8
100
Plevel = 0 dBm
Power splitter
R137
16
R39
R1
6 dB loss
Plevel = -6 dBm
50 Ohm
Text on Board :
Coupled output -6 dBm
J4
SMA Connector Vertical Mixed Mount
C33
10nF
From AXTAL
J5
SMA Connector Vertical Mixed Mount
Plevel = 16 dBm
C34
10nF
5V_PLL
R15
4.7K
Pull low for int input
normal usage
J30
jmp2
ISO_100MHZ_EXT_INT
Coupled_CLK
To FPGA CLK Shaper and galvanic isolator
rev.
by
notes
100MHz in the loop v3.0
Project : ET Pathfinder Demonstrator
Sheetname : OCXO_ASY
11500.04.02.3
Designed by
G. Visser & P. Jansweijer
Drawn by
G. Visser & P. Jansweijer
Size 420 x 297mm
Sheet 12 of 21 A3
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Place all componest under the shielded can, to shield it from EMI, and reduce the airflow around this circuit

Vtune = 0 to 5V (Guaranteed 0V22 - 4V75)

0-5V

7V9 @ 10mA

5V @ 1mA

Route the Vtune OCXO,short as possible to the OCXO.
The circuit in this box should be close as possible at the OCXO.
Vtune = 0 to 10V (Guaranteed 0V22 - 10V)

Slots in the board

LTC6655BHLS8-5.0

rev.	by	notes

100MHz in the loop v3.0

Project : ET Pathfinder Demonstrator

Sheetname : OCXO_DAC

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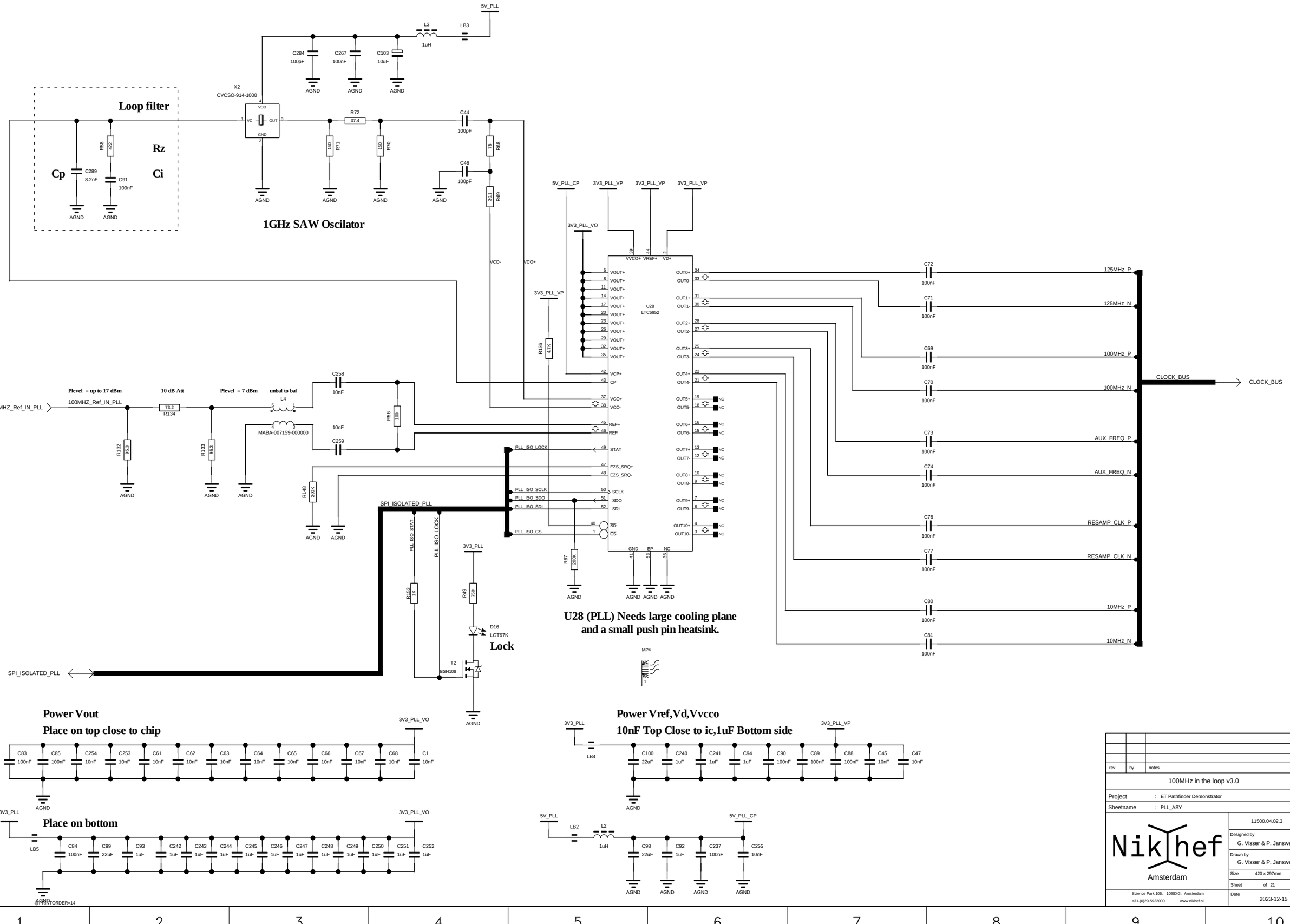
Size: 420 x 297mm

Sheet: 13 of 21 | A3

Date: 2023-12-15



rev.	by	notes

100MHz in the loop v3.0

Project : ET Pathfinder Demonstrator

Sheetname : PLL_ASY

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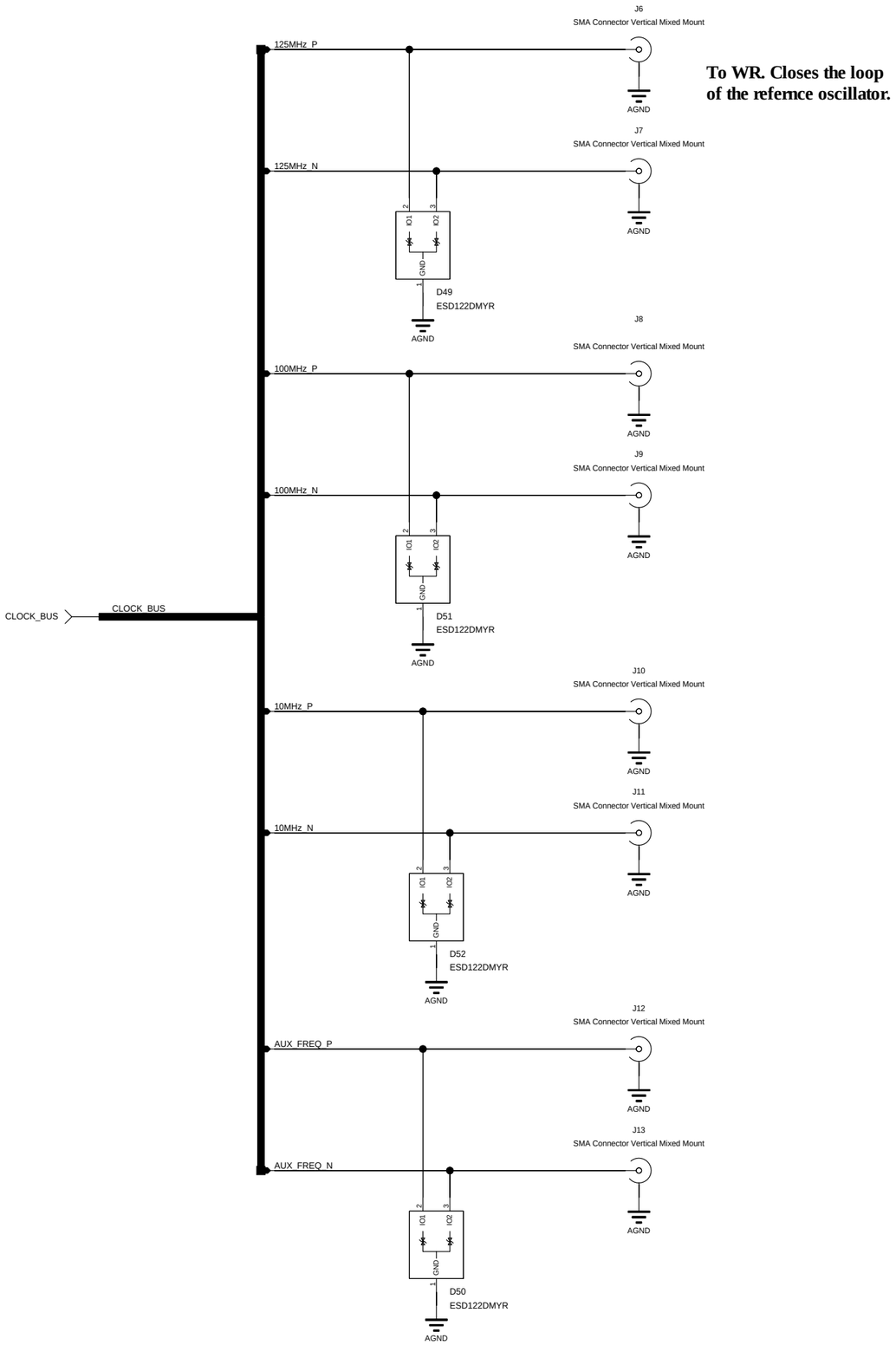
Size: 420 x 297mm

Sheet of 21 A3

Date: 2023-12-15



To WR. Closes the loop of the refernce oscillator.

rev.	by	notes

100MHz in the loop v3.0

Project : ET Pathfinder Demonstrator

Sheetname : Clock_Out_Connectors

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Size 420 x 297mm

Sheet 15 of 21 A3

Date 2023-12-15

CLOCKS From WR
Phase aligned with WR
125 MHz reference clock.

J14
SMA Connector Vertical Mixed Mount
AGND
CLK_FROM_WR_P

J15
SMA Connector Vertical Mixed Mount
AGND
CLK_FROM_WR_N

D53
ESD122DMYR
AGND

1 PPS DC coupled!

J16
SMA Connector Vertical Mixed Mount
AGND
1PPS_FROM_WR_P

J17
SMA Connector Vertical Mixed Mount
AGND
1PPS_FROM_WR_N

D54
ESD122DMYR
AGND

J60
SMA Connector Vertical Mixed Mount
AGND
CLK_FROM_WR_2_P

J61
SMA Connector Vertical Mixed Mount
AGND
CLK_FROM_WR_2_N

D62
ESD122DMYR
AGND

J18
SMA Connector Vertical Mixed Mount
AGND
TEST_INPUT_P

J19
SMA Connector Vertical Mixed Mount
AGND
TEST_INPUT_N

D55
ESD122DMYR
AGND

CLOCK_BUS

CLOCKS_WR
CLOCK_BUS

Resampler
Sheet 17
CLOCKS_WR
CLOCK_BUS
CLOCKS_WR_RESAMPLED
CLOCKS_WR_RESAMPLED_SPARE

CLOCKS_WR_RESAMPLED
CLOCKS_WR_RESAMPLED_SPARE

Resampled Clk and
1 PPS from WR

J20
SMA Connector Vertical Mixed Mount
AGND
CLK_FROM_WR_RESAMPLED_P

Clk is AC
coupled CML!

J21
SMA Connector Vertical Mixed Mount
AGND
CLK_FROM_WR_RESAMPLED_N

D56
ESD122DMYR
AGND

J22
SMA Connector Vertical Mixed Mount
AGND
1PPS_FROM_WR_RESAMPLED_P

1 PPS is LVPECL
DC Coupled!

J23
SMA Connector Vertical Mixed Mount
AGND
1PPS_FROM_WR_RESAMPLED_N

D57
ESD122DMYR
AGND

J26
SMA Connector Vertical Mixed Mount
AGND
CLK_FROM_WR_RESAMPLED_2_P

J27
SMA Connector Vertical Mixed Mount
AGND
CLK_FROM_WR_RESAMPLED_2_N

D59
ESD122DMYR
AGND

J24
SMA Connector Vertical Mixed Mount
AGND
RESAMPLER_CLK_SPARE0_P
C209
100nF

J25
SMA Connector Vertical Mixed Mount
AGND
RESAMPLER_CLK_SPARE0_N
C210
100nF

D58
ESD122DMYR
AGND

rev.	by	notes

100MHz in the loop v3.0

Project : ET Pathfinder Demonstrator
Sheetname : WR_CLOCKS_IO

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Drawn by G. Visser & P. Jansweijer
Size 420 x 297mm
Sheet 16 of 21 A3
Date 2023-12-15

CLOCKS From WR

CLOCKS_WR

CLOCKS_WR

CLOCK_BUS

CLOCK_BUS

283 mA

LB15

C154 47uF

C137 100nF

C322 1nF

D60 HMC6832ALP5LE

AGND

Propagation Delay : 207 ps

3V3_RESAMPLERS

LB13

Resampler MHz D FLIP FLOP

C101 22uF

C95 1uF

C127 100nF

C285 100pF

R108 10

AGND

C128 100nF

C106 10uF

C286 100pF

AGND AGND AGND

CLK_FROM_WR_P

CLK_FROM_WR_N

RESAMPLER_CLK0_P

RESAMPLER_CLK0_N

C131 100nF

C132 100nF

C129 100nF

C130 100nF

U24 HMC747LC3C

VCC VCC VR

DP DN CP CN

D Clk Q Q'

QP QN

GND GND GND GND GND GND GND EP

1 4 5 8 9 12 14 EP

C133 100nF

C134 100nF

AGND

OnChip Termination

3V3_RESAMPLERS

LB23

Resampler MHz D FLIP FLOP

C207 22uF

C206 1uF

C218 100nF

C288 100pF

R129 10

AGND

C211 100nF

C208 10uF

C287 100pF

AGND AGND AGND

CLK_FROM_WR_2_P

CLK_FROM_WR_2_N

RESAMPLER_CLK2_P

RESAMPLER_CLK2_N

C214 100nF

C215 100nF

C212 100nF

C213 100nF

U27 HMC747LC3C

VCC VCC VR

DP DN CP CN

D Clk Q Q'

QP QN

GND GND GND GND GND GND GND EP

1 4 5 8 9 12 14 EP

C216 100nF

C217 100nF

CLK_FROM_WR_RESAMPLED_2_P

CLK_FROM_WR_RESAMPLED_2_N

AGND

OnChip Termination

CLK_FROM_WR_RESAMPLED_P

CLK_FROM_WR_RESAMPLED_N

Resampeled clk from WR

CLOCKS_WR_RESAMPLED

CLOCKS_WR_RESAMPLED

3V3_RESAMPLERS

LB14

U25 LM1117MP-2.5

IN OUT GND

C96 1uF

C135 100nF

C136 100nF

C102 22uF

AGND AGND AGND AGND AGND

Resampler 1 PPS D FLIP FLOP

R120 10K

R122 10K

Resampeled 1 PPS from WR

1PPS_FROM_WR_P

1PPS_FROM_WR_N

R12 100

U26 MAX9381

VCC D D Q Q CLK CLK VEE

1PPS_FROM_WR_RESAMPLED_P

1PPS_FROM_WR_RESAMPLED_N

Resampler clocks

RESAMP_CLK_P

RESAMP_CLK_N

R10 100

AGND

D60 HMC6832ALP5LE

CLOCK BUFFER

CONFIG IN_SEL INP0 INN0 INP1 INN1 VAC_REF

OUTP0 OUTN0 OUTP1 OUTN1 OUTP2 OUTN2 OUTP3 OUTN3 OUTP4 OUTN4 OUTP5 OUTN5 OUTP6 OUTN6 OUTP7 OUTN7

NC

LVPECL pairs should be delay matched

RESAMPLER_CLK0_P

RESAMPLER_CLK0_N

RESAMPLER_CLK1_P

RESAMPLER_CLK1_N

RESAMPLER_CLK2_P

RESAMPLER_CLK2_N

RESAMPLER_CLK_SPARE0_P

RESAMPLER_CLK_SPARE0_N

TEST_INPUT_P

TEST_INPUT_N

C138 100nF

C139 100nF

R13 100

3V3_RESAMPLERS

R44 10K

J33

jmp2 2 1

Default Place Jumper => Select IN0

AGND

R118 150

R117 150

R116 150

R115 150

R114 150

R113 150

R111 150

R112 150

AGND AGND AGND AGND AGND AGND AGND AGND

CLK_RESAMPERS

RESAMPLER_CLK1_P

RESAMPLER_CLK1_N

C140 100nF

C141 100nF

R11 100

R119 10K

R121 10K

AGND AGND

R109 91

R110 91

AGND AGND AGND

CLOCKS_WR_RESAMPLED_SPARE

CLOCKS_WR_RESAMPLED_SPARE

rev.	by	notes
		100MHz in the loop v3.0

Project : ET Pathfinder Demonstrator

Sheetname : RESAMPER

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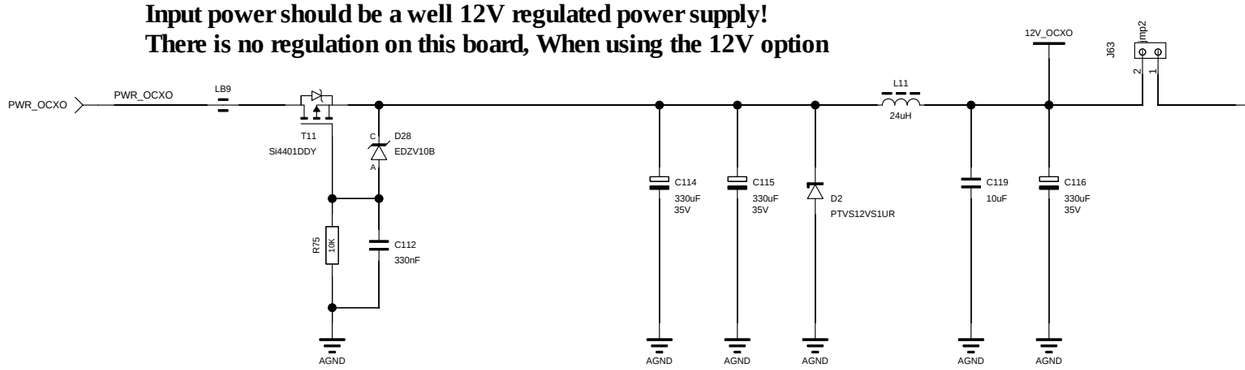
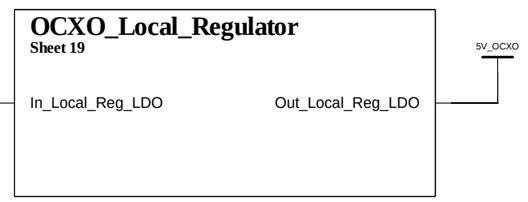
Sheet 17 of 21 A3

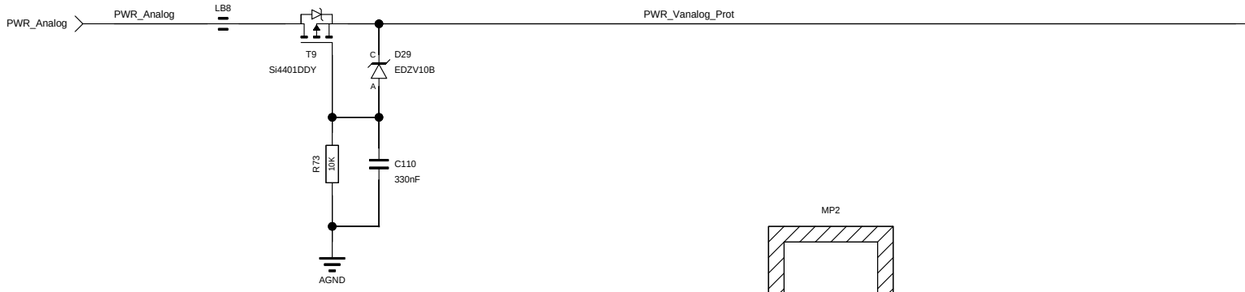
Date 2023-12-15

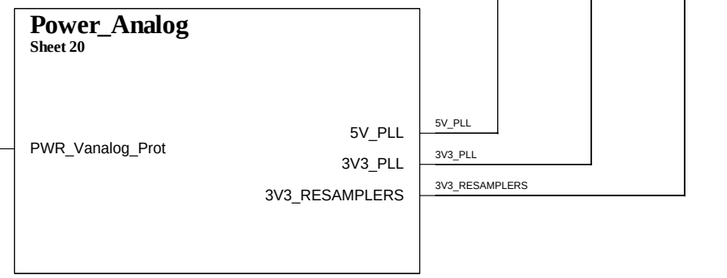
Input power should be a well 12V regulated power supply!
There is no regulation on this board, When using the 12V option

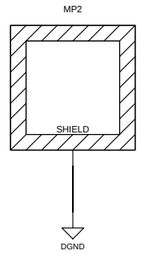




Max voltage 6V5

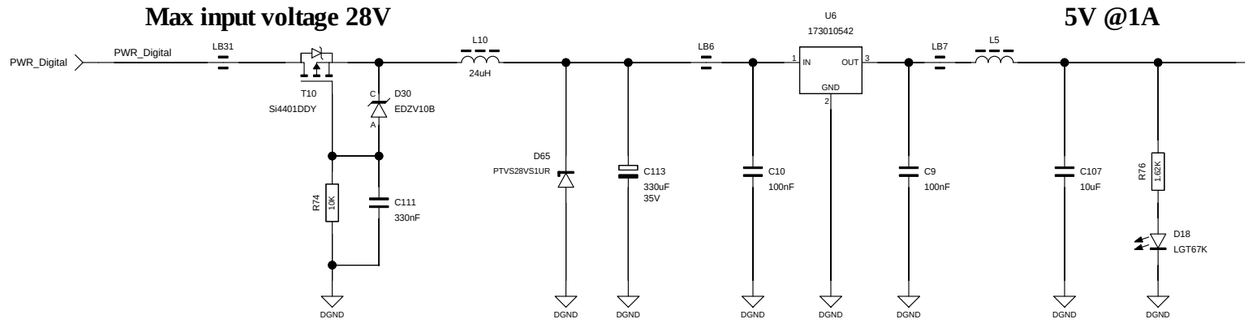


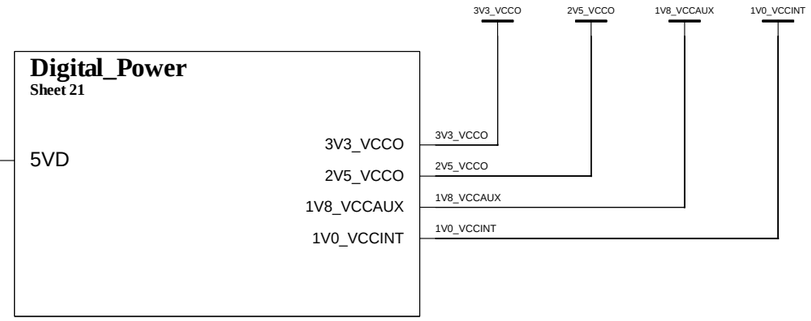




Max input voltage 28V

5V @1A





rev.	by	notes

100MHz in the loop v3.0

Project : ET Pathfinder Demonstrator

Sheetname : Power

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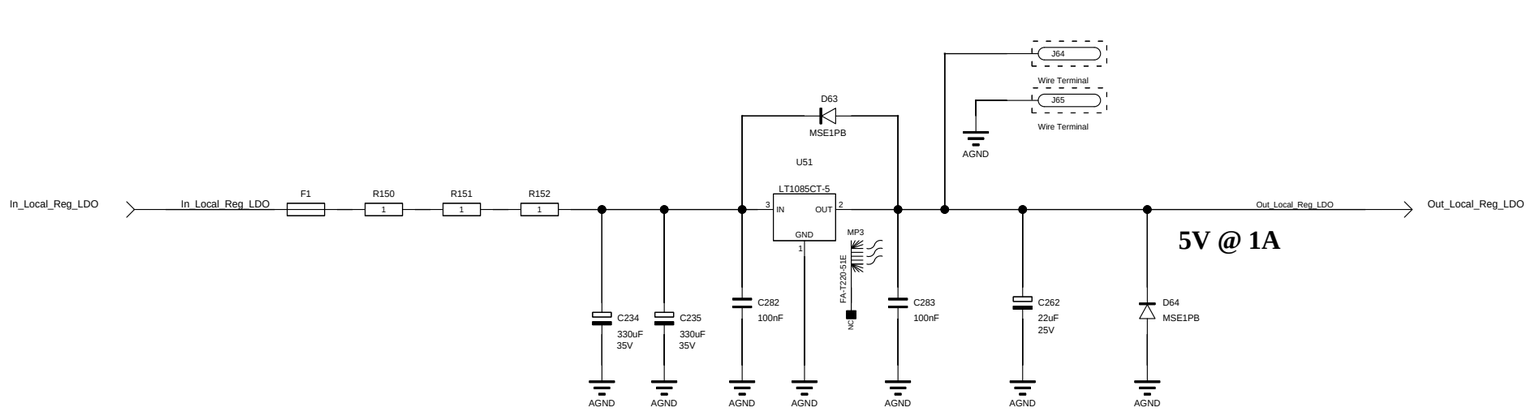
Size: 420 x 297mm

Sheet: 18 of 21 A3

Date: 2023-12-15

Todo:
MP3, replace FA-T220-64E (1006934) for FA-T220-51E (1007644)
https://redmine.nikhef.nl/et/issues/1273



Add TO220 isolation

rev.	by	notes

100MHz in the loop v3.0

Project : ET Pathfinder Demonstrator

Sheetname : OCXO_Local_Regulator

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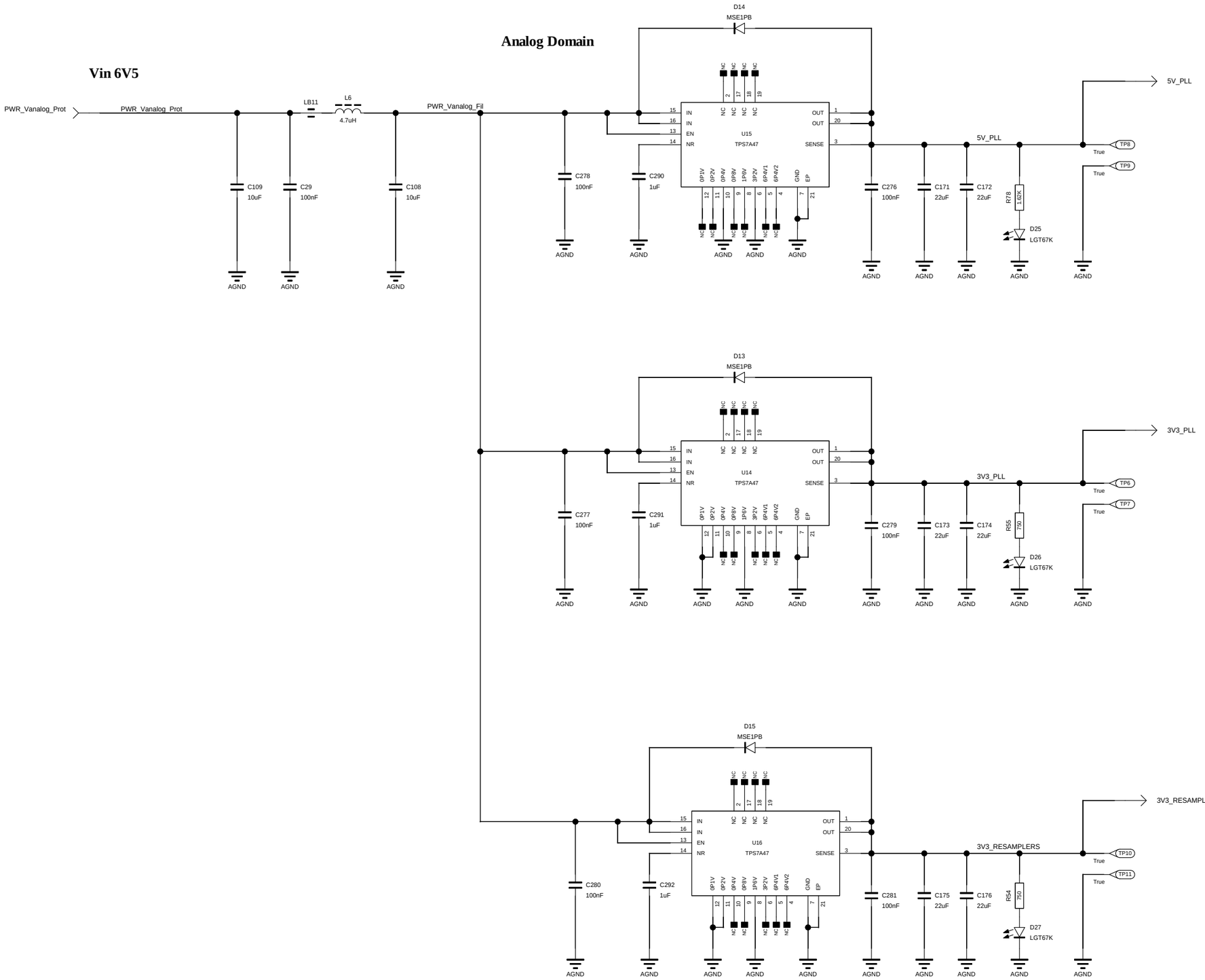
Date 2023-12-15

Analog Domain

Vin 6V5



rev.	by	notes

100MHz in the loop v3.0

Project : ET Pathfinder Demonstrator

Sheetname : Power_Analog

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Sheet: 20 of 21 A3

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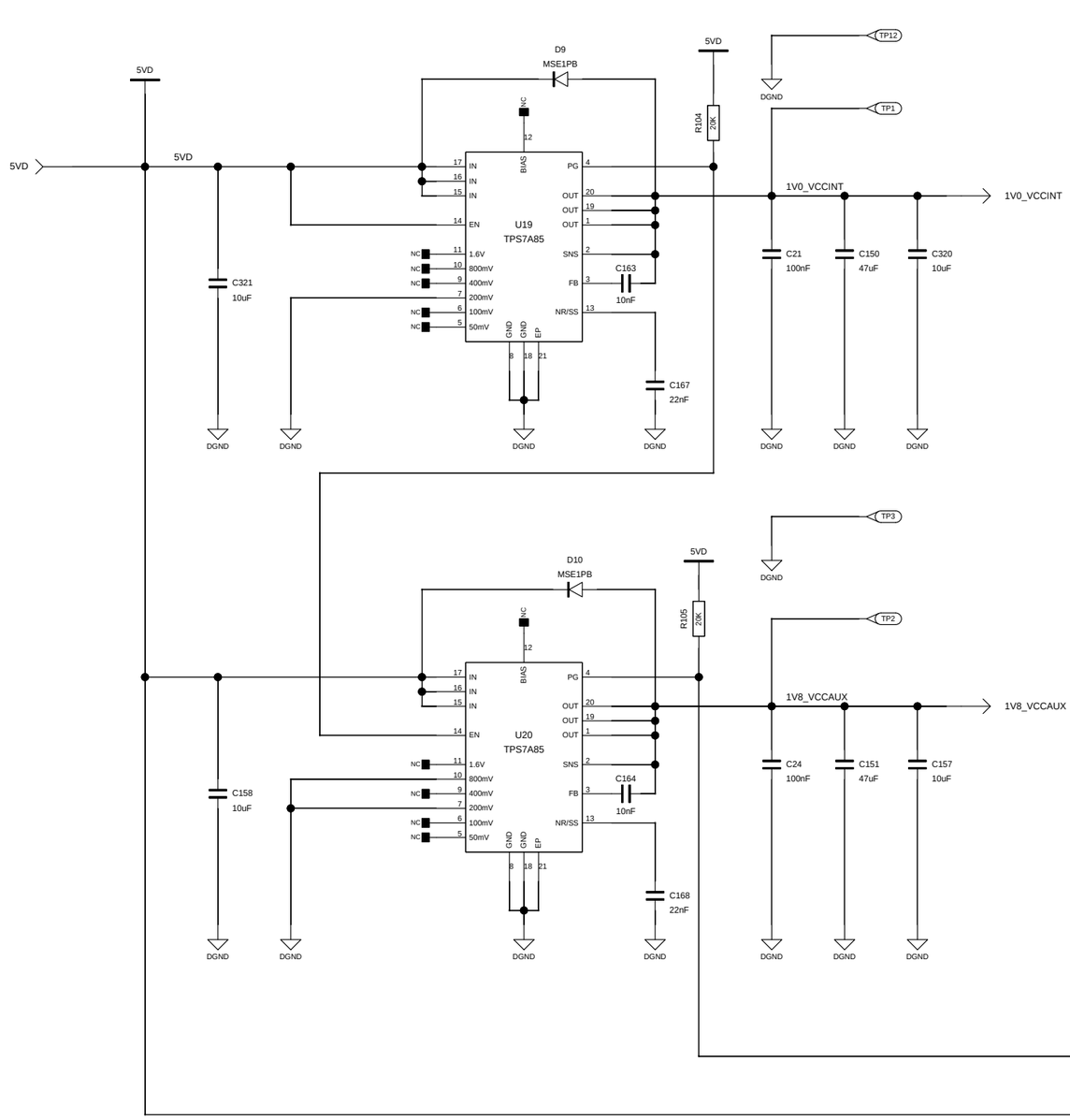

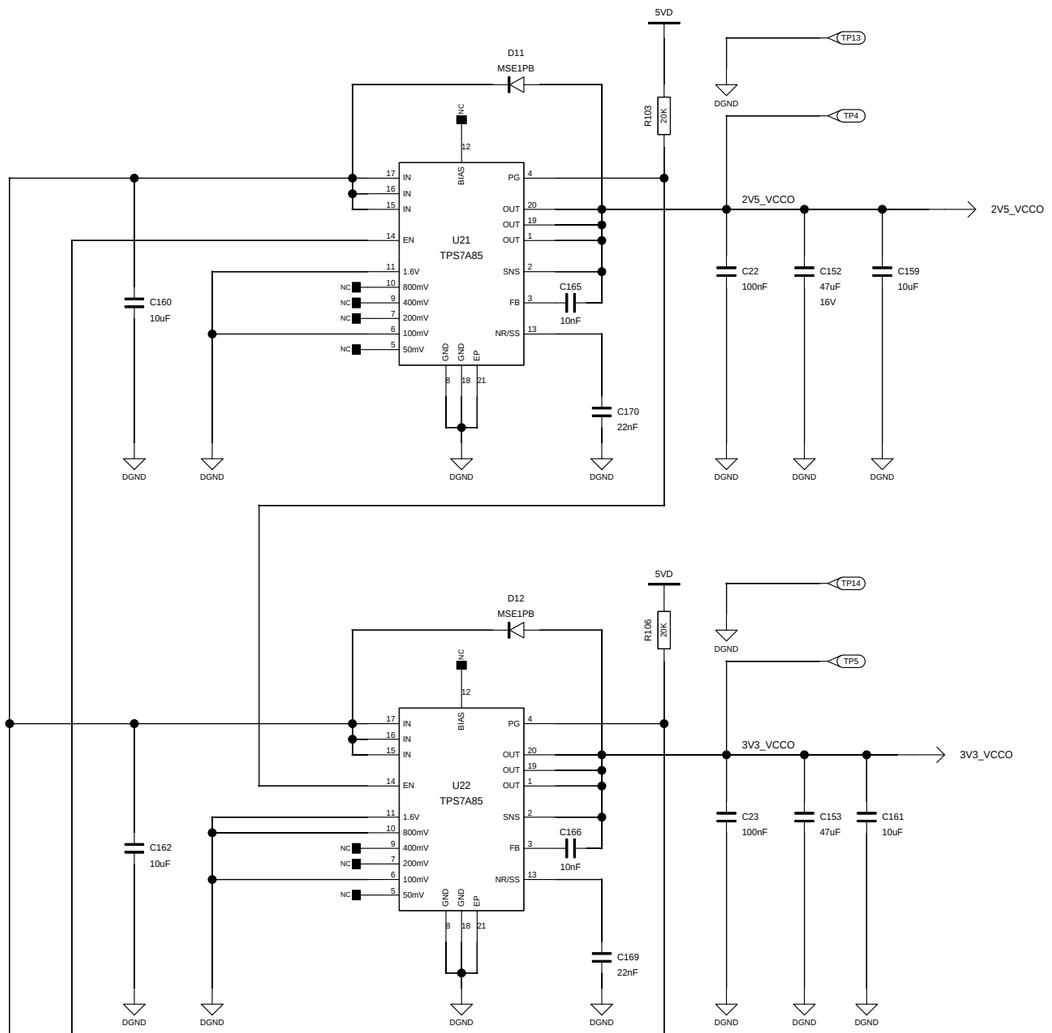

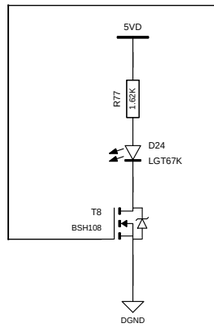

Power Oke

Powersupply for the FPGA.
The generated rail voltages are sequenced.
Sequence: 1V0 > 1V8_AUX > 2V5_VCCO > 3V3_VCCO

rev.	by	notes

100MHz in the loop v3.0

Project : ET Pathfinder Demonstrator
Sheetname : Digital_Power

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