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100MHz in the loop v3.0

Project : ET Pathfinder Demonstrator

Sheetname : Schematic1

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| | | 100MHz in the loop v3.0 |

Project : ET Pathfinder Demonstrator

Sheetname : WR_CLOCKS_IO

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Project : ET Pathfinder Demonstrator

Sheetname : RESAMPER

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**To WR. Closes the loop of the refernce oscillator.**

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100MHz in the loop v3.0

Project : ET Pathfinder Demonstrator

Sheetname : Clock_Out_Connectors

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# Connectors PLL Control & DAC

**Reducing common mode noise around 100 MHZ**

# Text on Board => LVDS !

**From WR. Tune Reference oscillator.**

**Reducing common mode noise around 100 MHZ**

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100MHz in the loop v3.0

Project : ET Pathfinder Demonstrator

Sheetname : Digital_IO

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**Test connector to hookup a microcrontroller.**
**LVCMOS 3V3! No buffers direct to the FPGA.**

**Spare IO can be used for various functions**
**depends on the firmware.**
**Signal direction depends on firmware**

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100MHz in the loop v3.0

Project : ET Pathfinder Demonstrator

Sheetname : External_SPI_test_Con

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**UG470 Table 2-1**

| Configuration mode | M2 | M1 | M0 | Bush With |
|---|---|---|---|---|
| Master Serial | 0 | 0 | 0 | x1 |
| Master SPI | 0 | 0 | 1 | x1,x2,x4 |
| Master BPI | 0 | 1 | 0 | x8,x16 |
| | 0 | 1 | 1 | |
| Master SelectMap | 1 | 0 | 0 | x8,x16 |
| JTAG | 1 | 0 | 1 | x1 |
| Slave SelectMap | 1 | 1 | 0 | x8,x16,x32 |
| Slave Serial | 1 | 1 | 1 | x1 |

**ESD protection**

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100MHz in the loop v3.0

Project : ET Pathfinder Demonstrator

Sheetname : FPGA_EEPROM_AND_JTAG

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100MHz in the loop v3.0

Project : ET Pathfinder Demonstrator

Sheetname : FPGA_Spartan7

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**UG483 Table 2-1 (XC7S50 FTGB196):**
**VCCINT: 1x 100uF, 3x 4.7uF, 5x 0.47uF**
**VCCBRAM: 1x 100uF, 1x 47uF, 1x 4.7uF, 1x 0.47uF**
**VCCAUX: 1x 47uF, 1x 4.7uF, 3x 0.47uF**
**VCCO: 1x 47uF, 2x 4.7uF, 4x 0.47uF**

**DS189 Table 2 note 9**
**If battery is not used, connect VCCBATT to either ground or VCCAUX**

**UG480 Figure 1-2**
**ADC is not used in this desgin**

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100MHz in the loop v3.0

Project : ET Pathfinder Demonstrator
Sheetname : FPGA_POWER

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100MHz in the loop v3.0

Project : ET Pathfinder Demonstrator

Sheetname : FPGA_BANK_14_34

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**CFGBVS Pulled to 3V3 this pin selects the voltage IO for bank 0**
**See UG470 7 Series config guide Table 2-4**

**PROGRAM_B_0 (PROG) Active low reset.**
**When pulsed low the FPGA config is cleared and reloaded from FLASH.**

**See UG470 7 Series config guide Table 4-2**

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100MHz in the loop v3.0

Project : ET Pathfinder Demonstrator

Sheetname : FPGA_CONFIG

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100MHz in the loop v3.0

Project : ET Pathfinder Demonstrator

Sheetname : ISO_SPI_DAC_PLL

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FPGA clk Shaphing and isolating

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100MHz in the loop v3.0

Project : ET Pathfinder Demonstrator

Sheetname : CLK_SHAPER

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100MHz in the loop v3.0

Project : ET Pathfinder Demonstrator

Sheetname : OCXO_ASY

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Project : ET Pathfinder Demonstrator

Sheetname : OCXO_DAC

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Loop filter
CVCSO-914-1000
Cp
Rz
Ci
1GHz SAW Oscilator
U28 (PLL) Needs large cooling plane and a small push pin heatsink.
Lock
Power Vout
Place on top close to chip
Place on bottom
Power Vref,Vd,Vvcco
10nF Top Close to ic,1uF Bottom side
100MHz in the loop v3.0
Project : ET Pathfinder Demonstrator
Sheetname : PLL_ASY
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**Input power should be a well 12V regulated power supply!**
**There is no regulation on this board, When using the 12V option**

**Max voltage 6V5**

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100MHz in the loop v3.0

Project : ET Pathfinder Demonstrator

Sheetname : Power

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**Powersupply for the FPGA.**
**The generated rail voltages are sequenced.**
**Sequence: 1V0 > 1V8_AUX > 2V5_VCCO > 3V3_VCCO**

**Power Oke**

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100MHz in the loop v3.0

Project : ET Pathfinder Demonstrator

Sheetname : Digital_Power

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**Todo:**
**MP3, replace FA-T220-64E (1006934) for FA-T220-51E (1007644)**
**https://redmine.nikhef.nl/et/issues/1273**

**Add TO220 isolation**

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Project : ET Pathfinder Demonstrator
Sheetname : OCXO_Local_Regulator

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100MHz in the loop v3.0

Project : ET Pathfinder Demonstrator

Sheetname : Power_Analog

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100MHz in the loop v3.0

Project : ET Pathfinder Demonstrator

Sheetname : Switch_and_led

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