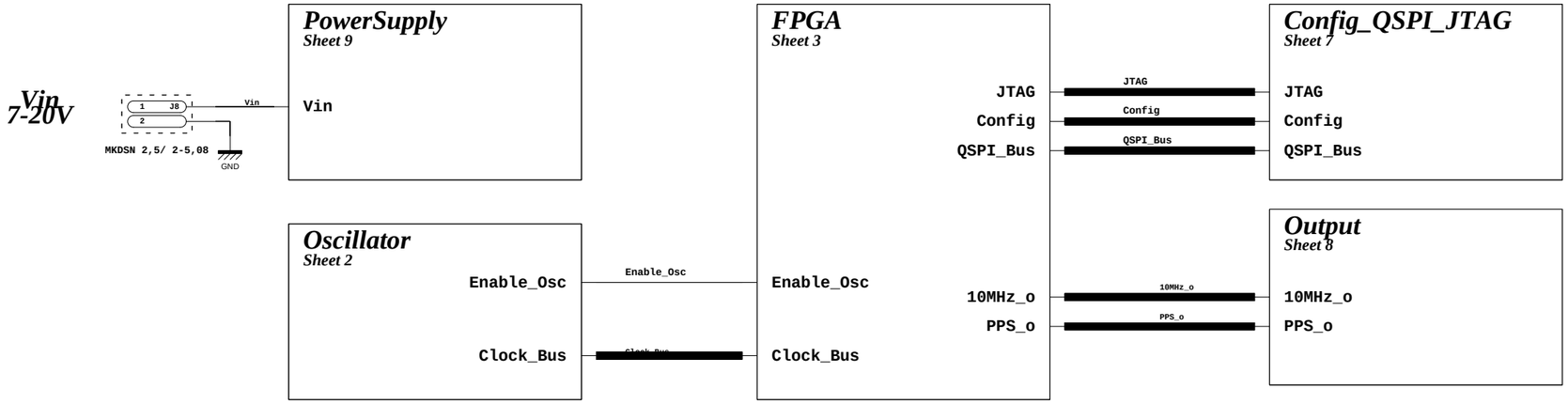

rev.	by	notes

Grand Master Source

Project : Timing

Sheetname : Schematic1

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Drawn by p. Jansweijer

Size 420 x 297mm

Sheet 1 of 9 A3

Date 2023 09 25

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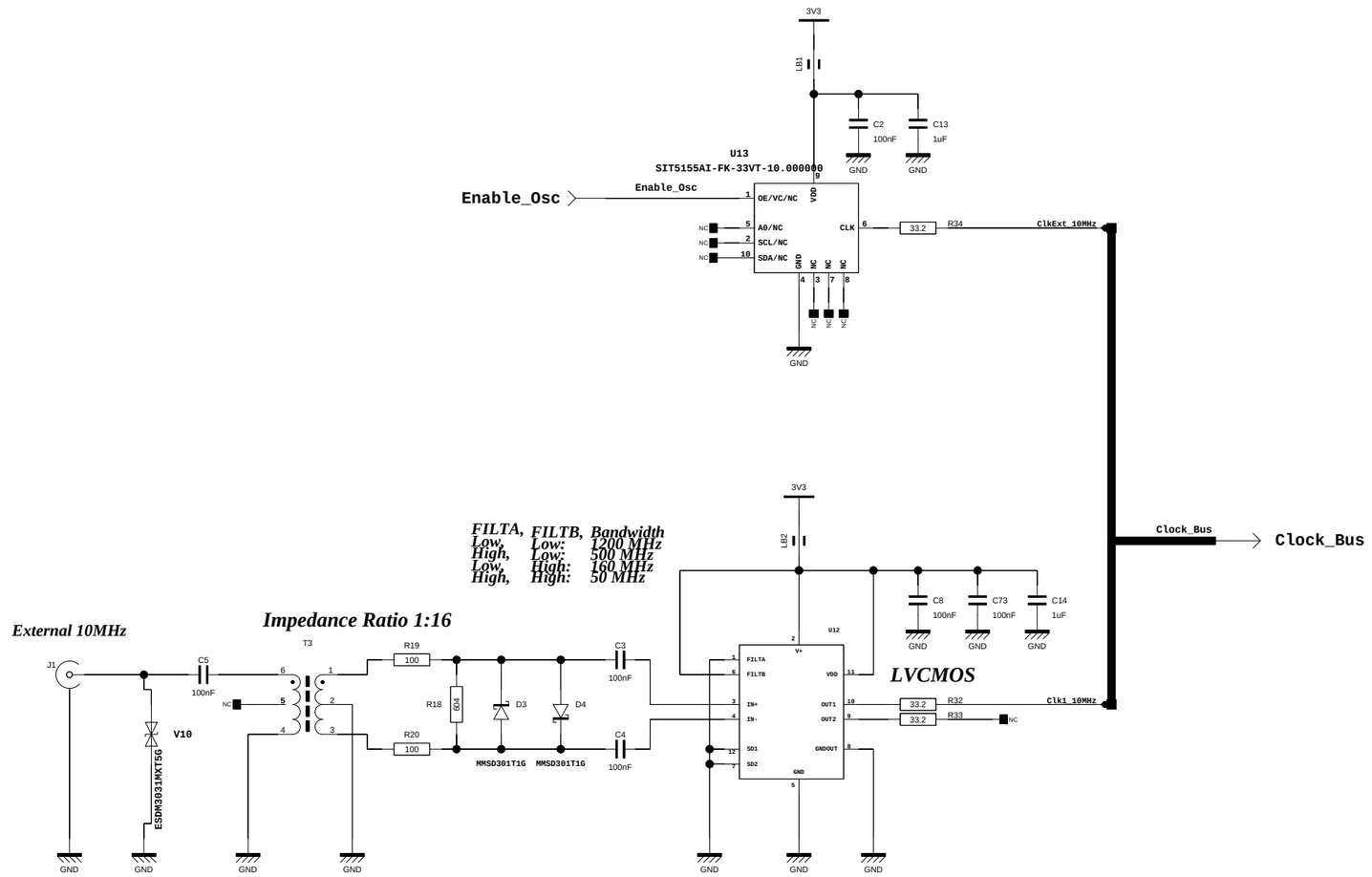

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Project : Timing

Sheetname : Oscillator

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Sheet: 2 of 9 A3

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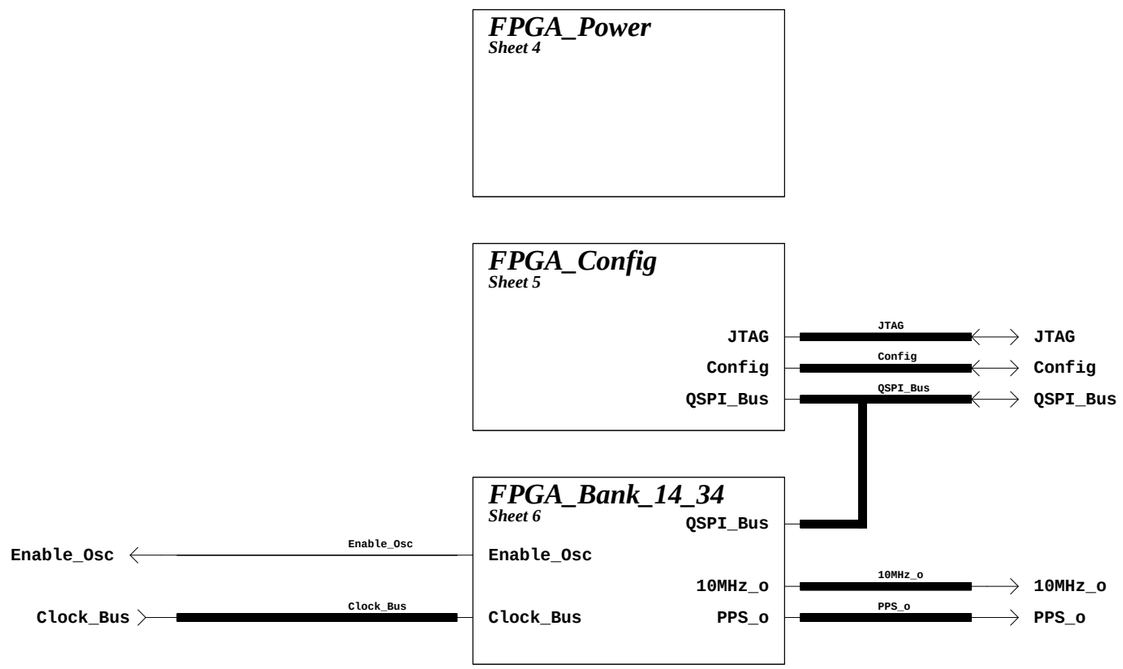

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Project : Timing

Sheetname : FPGA

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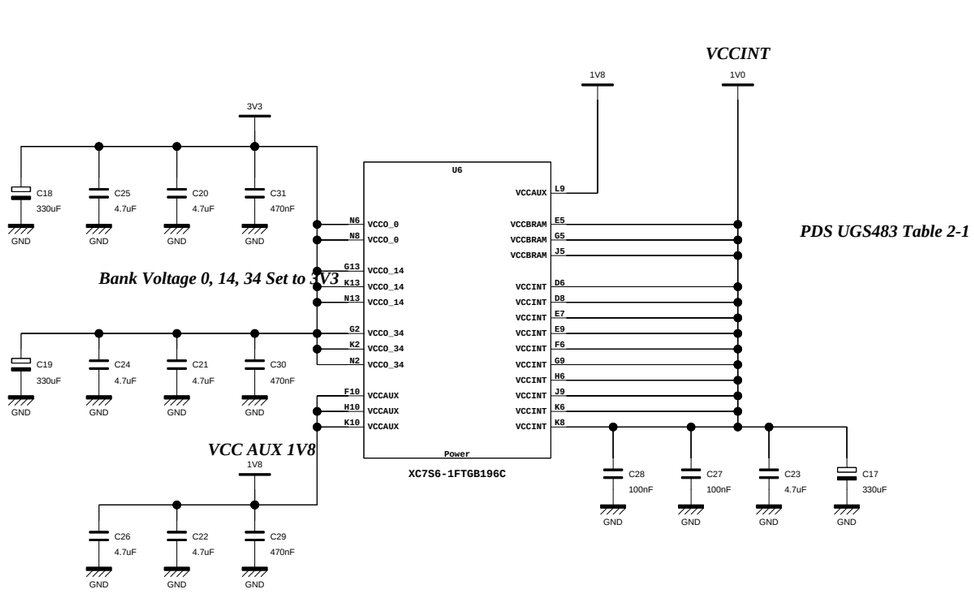
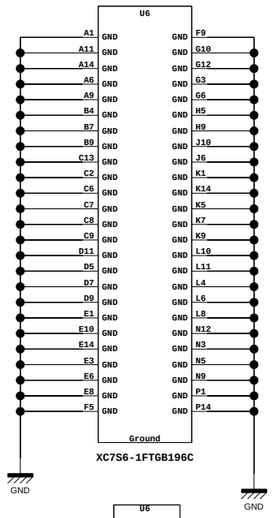
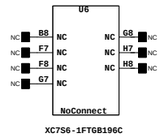


PDS UGS483 Table 2-1





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Project : Timing

Sheetname : FPGA_Power

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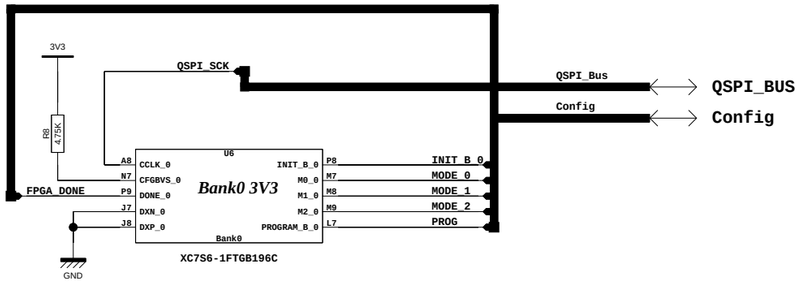
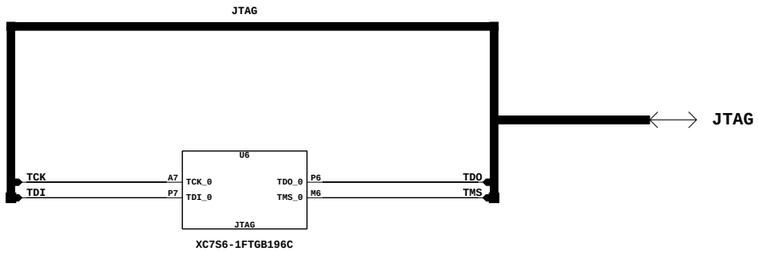
CFGBVS Pulled to 3V3 this pin selects the voltage IO for bank 0
See UG470 7 Series config guide Table 2-4





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Project : Timing

Sheetname : FPGA_Config

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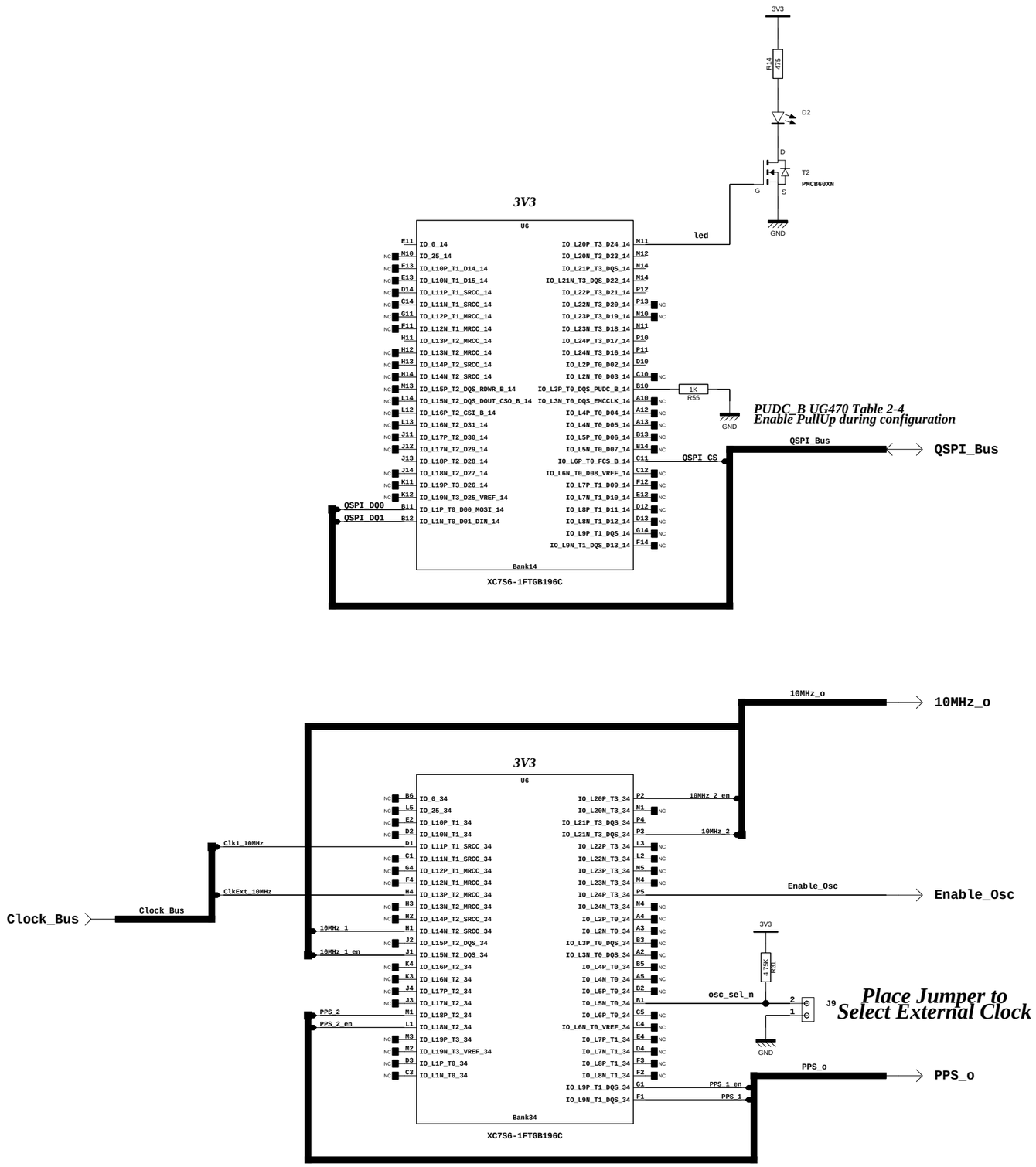

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Project : Timing

Sheetname : FPGA_Bank_14_34

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Sheet: 6 of 9 A3

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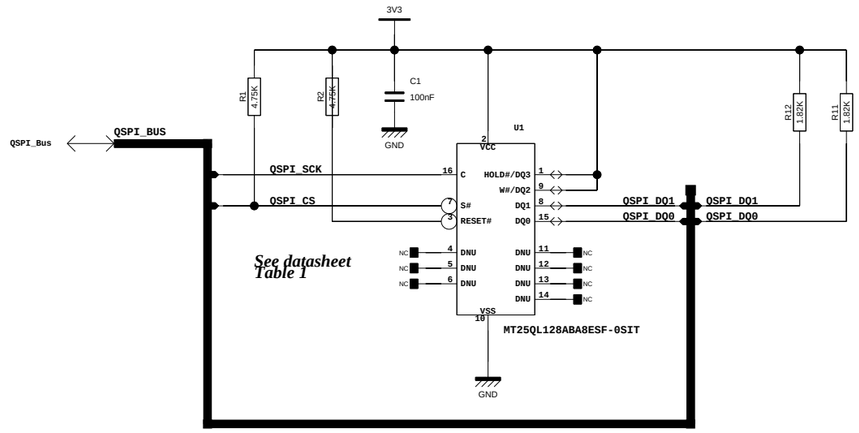
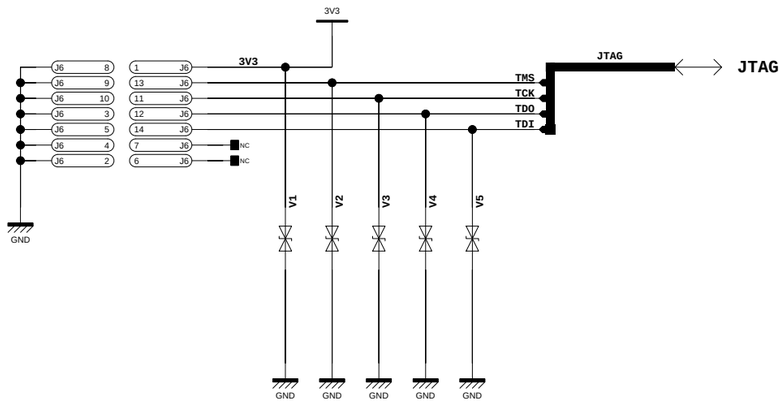
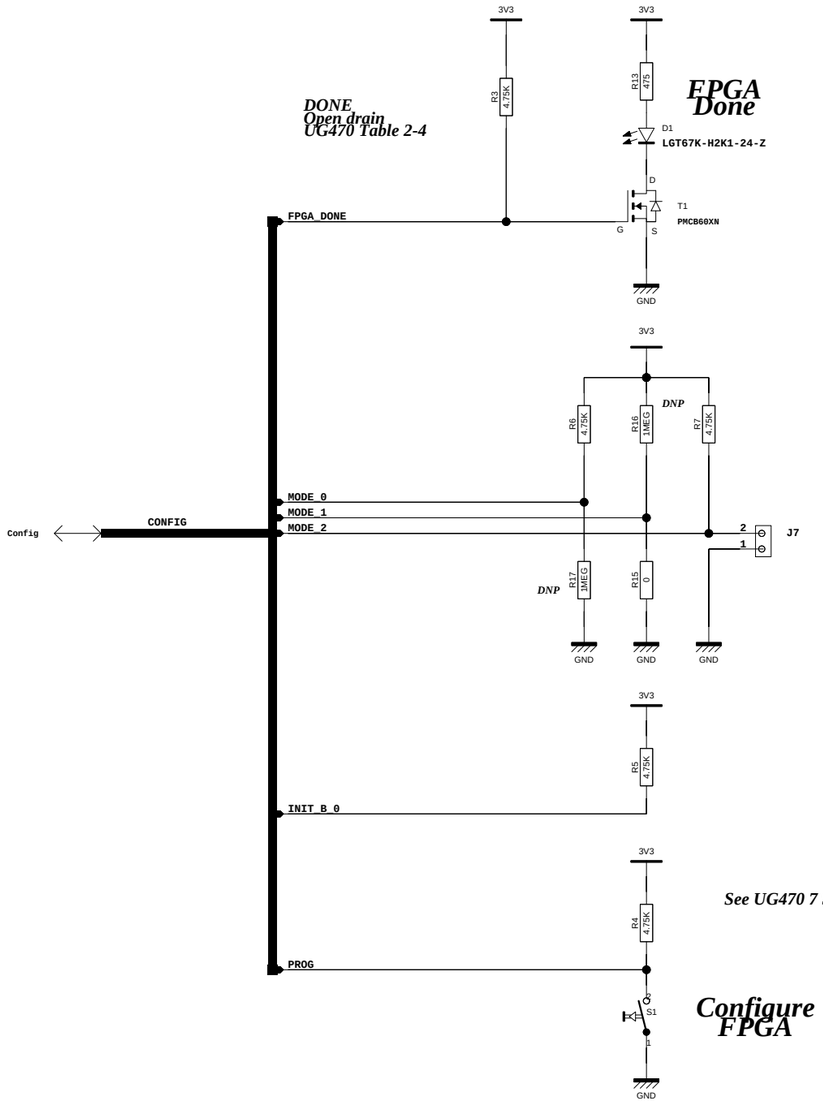




ESD protection



Configuration mode	M2	M1	M0	Bus Width
Master Serial	0	0	0	x1
Master SPI	0	0	1	x1,x2,x4
Master BPI	0	1	0	x8,x16
Master SelectMap	1	0	0	x8,x16
JTAG	1	0	1	x1
Slave SelectMap	1	1	0	x8,x16,x32
Slave Serial	1	1	1	x1

UG470 Table 2-1

Mode set to [M2:M0] 101 (JTAG Mode)
Place Jumper For 100 (FLASH BOOT)
UG470 Table 2-1

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Project : Timing

Sheetname : Config_QSPI_JTAG

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Sheet 7 of 9 A3

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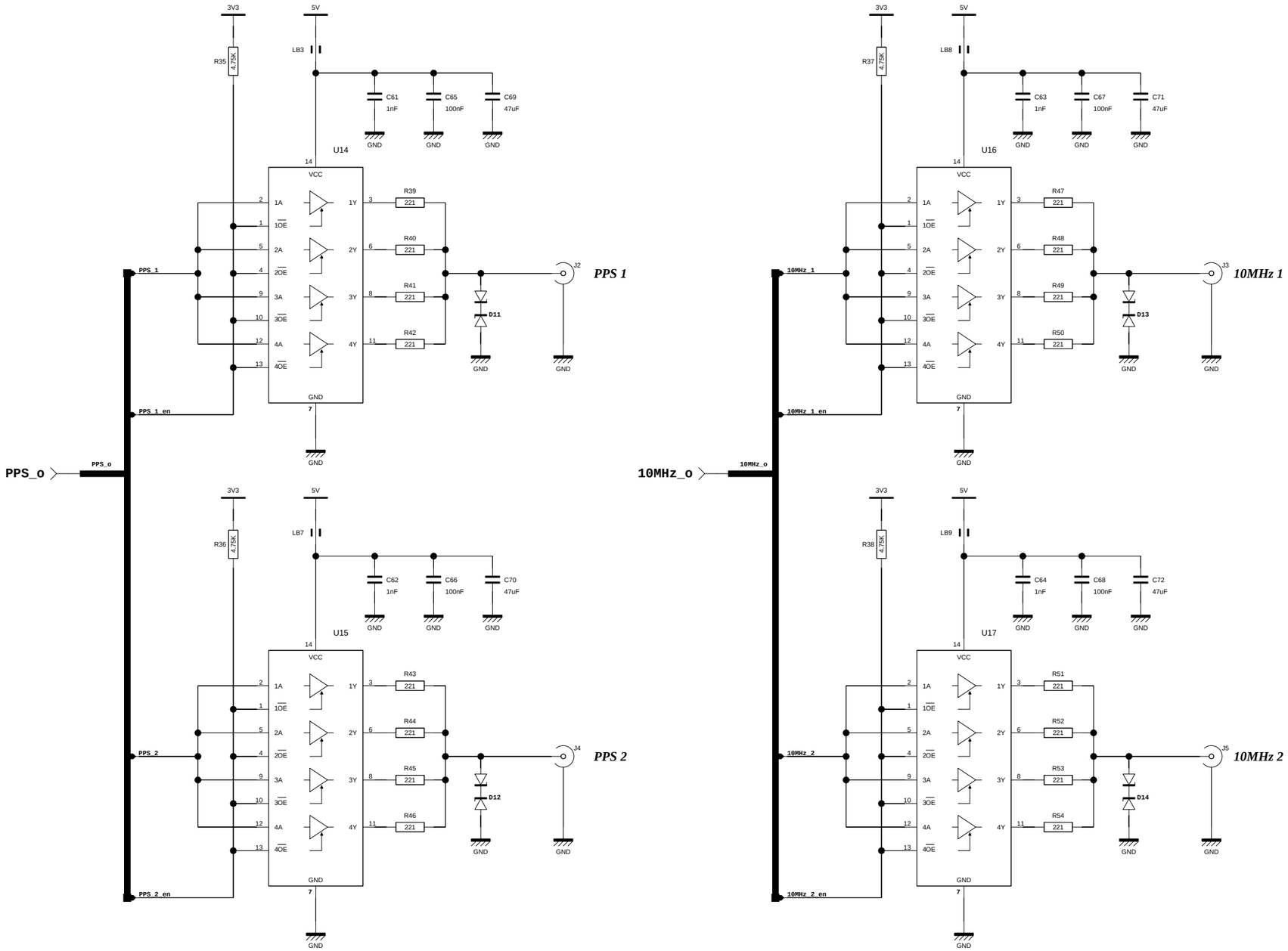

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Project : Timing

Sheetname : Output

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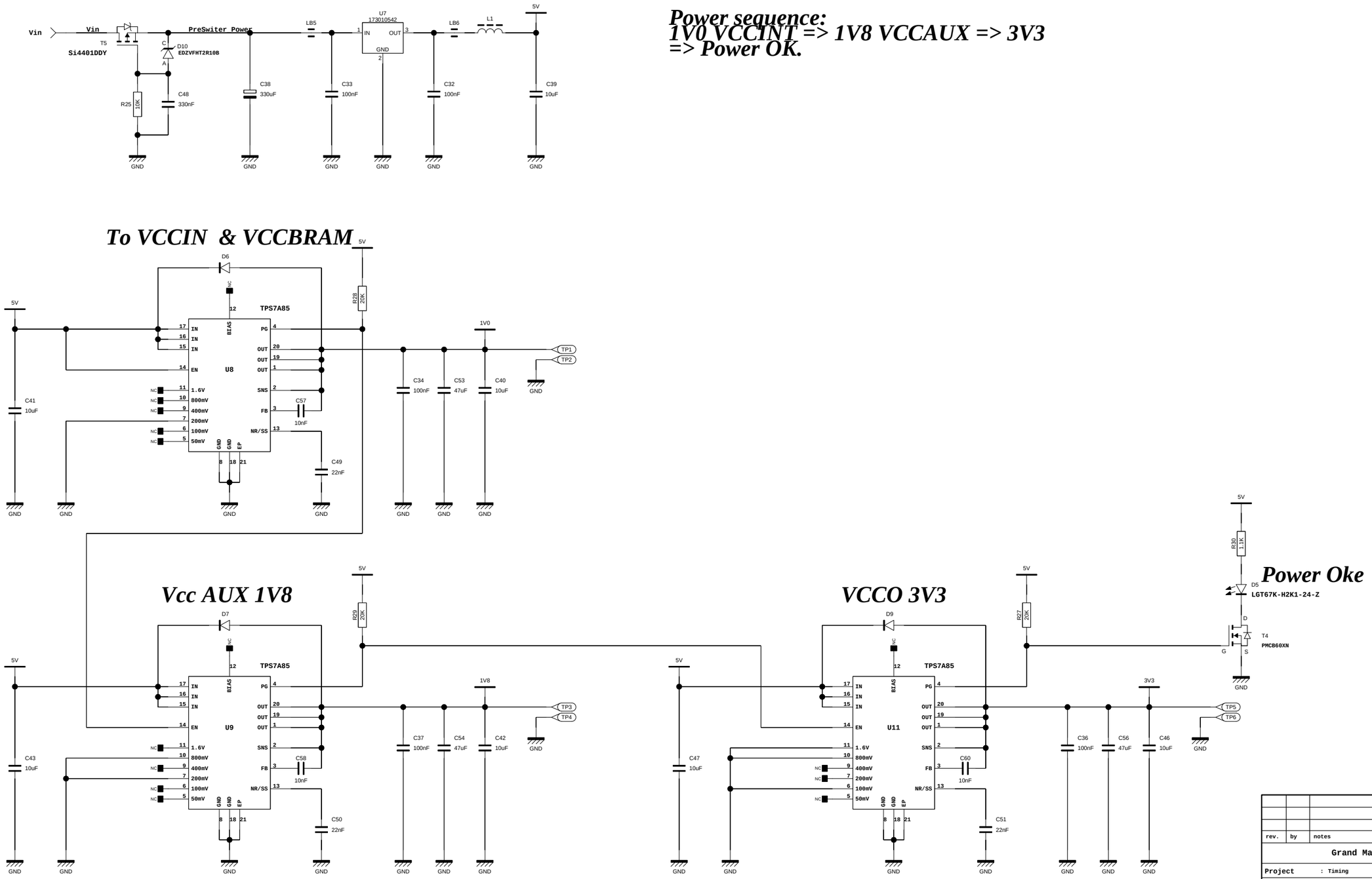
Sheet 8 of 9 A3

Date 2023 09 25



Power sequence:
1V0 VCCINT => 1V8 VCCAUX => 3V3
=> Power OK.

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Project : Timing

Sheetname : PowerSupply

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Sheet: 9 of 9 — A3

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