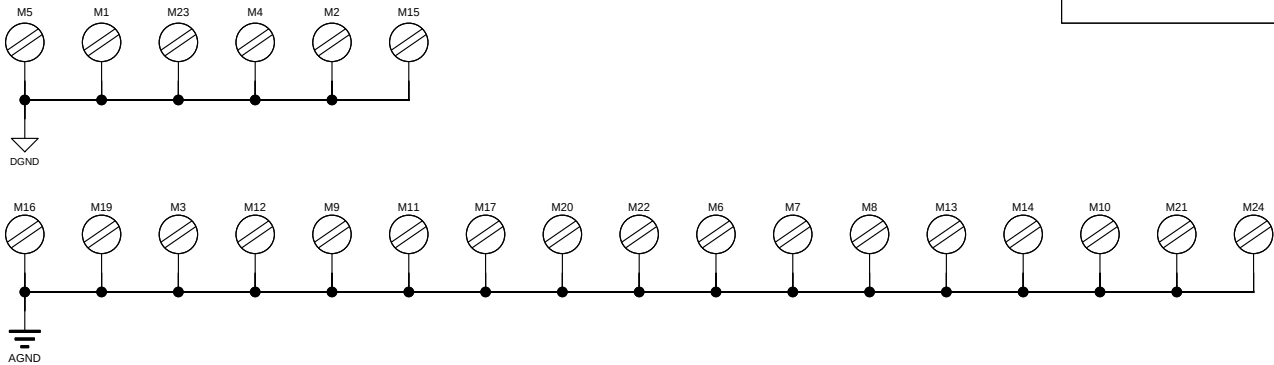
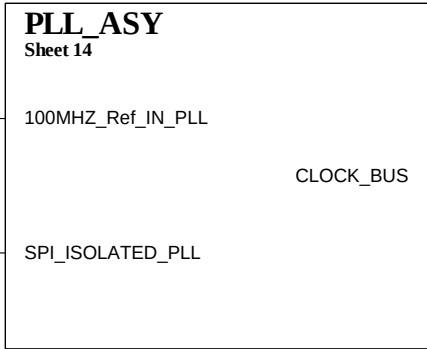
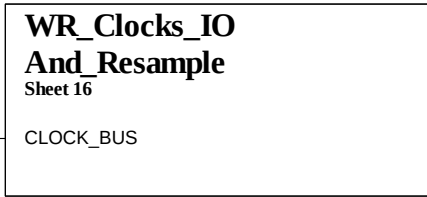
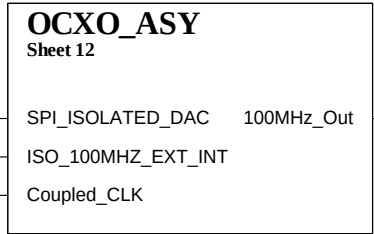
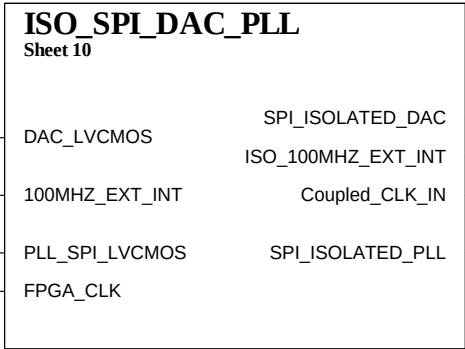
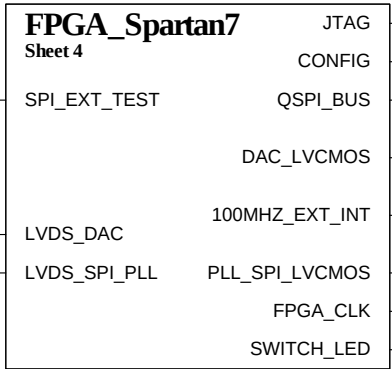
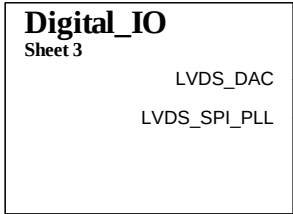
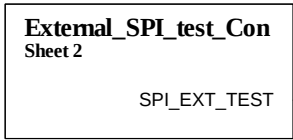
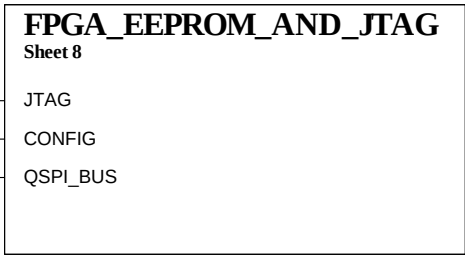
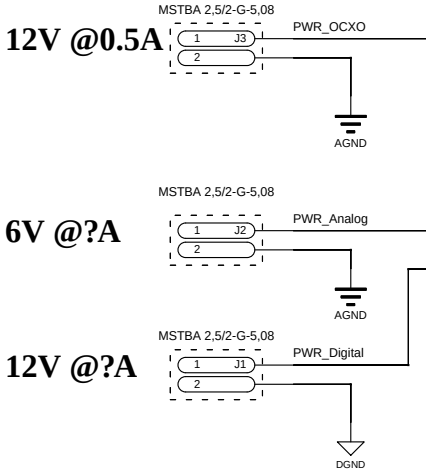
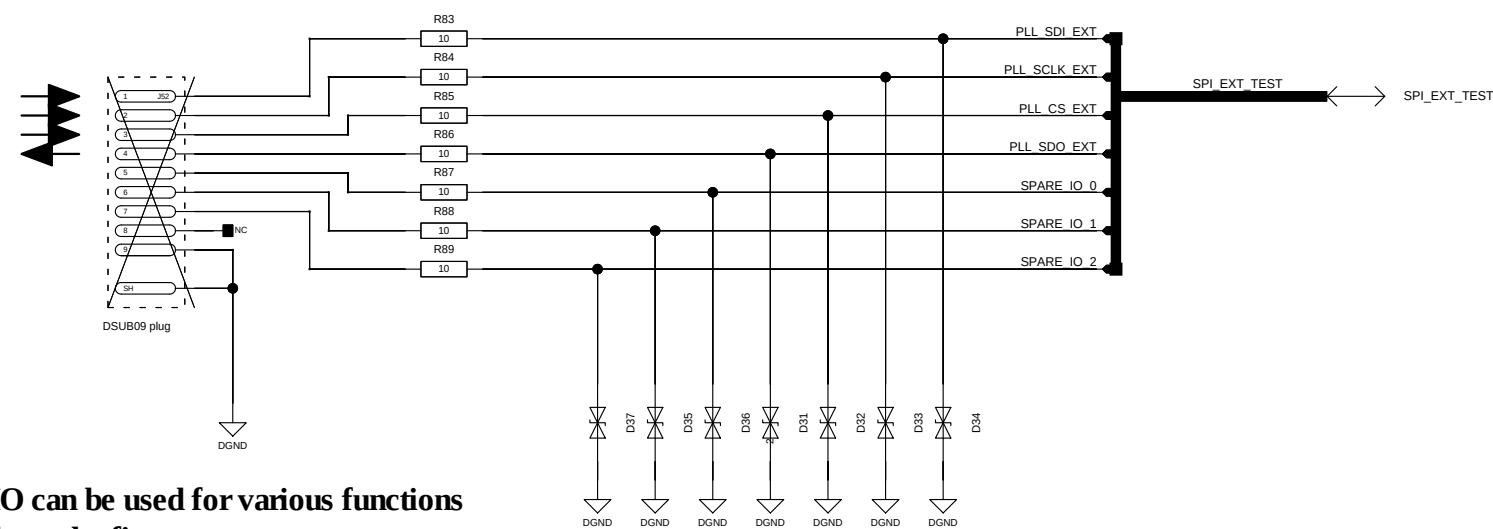


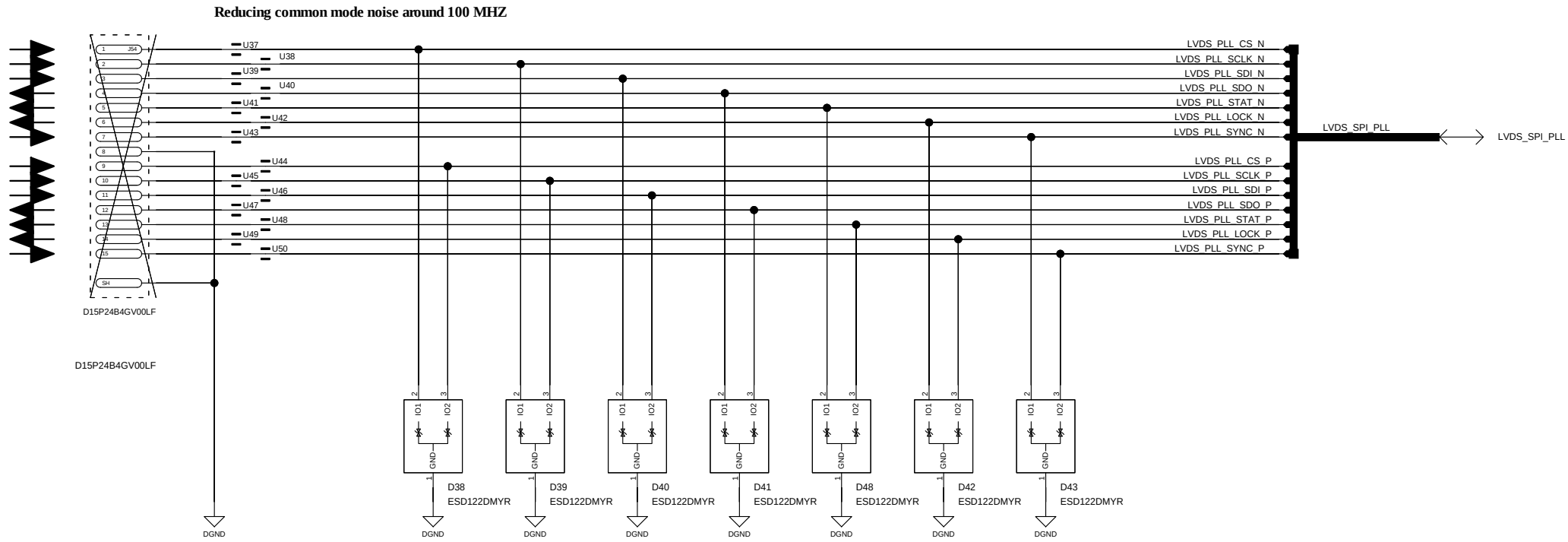


rev.	by	notes
100MHz in the loop v2.0		
Project : ET Pathfinder Demonstrator		
Sheetname : Schematic1		
		11500.04.02.2
		Designed by G. Visser & P. Jansweijer
		Drawn by G. Visser & P. Jansweijer
		Size 420 x 297mm
		Sheet 1 of 21 A3
Science Park 105, 1098XG, Amsterdam +31-(0)20-5922000 www.nikhef.nl		Date 2023-07-20



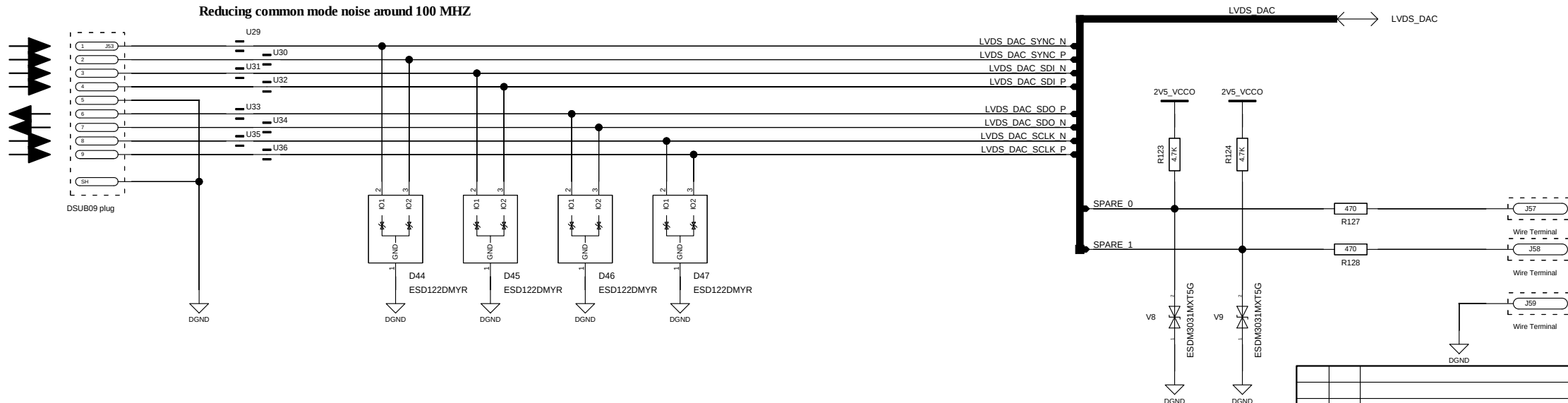
rev.	by	notes	
100MHz in the loop v2.0			
Project : ET Pathfinder Demonstrator			
Sheetname : External_SPI_test_Con			
 Nikhef Amsterdam		11500.04.02.2	
		Designed by G. Visser & P. Jansweijer	
		Drawn by G. Visser & P. Jansweijer	
		Size 420 x 297mm	
		Sheet 2 of 21	A3
		Date 2023-07-20	
Science Park 105, 1098XG, Amsterdam +31-(0)20-5922000 www.nikhef.nl			

Connectors PLL Control & DAC

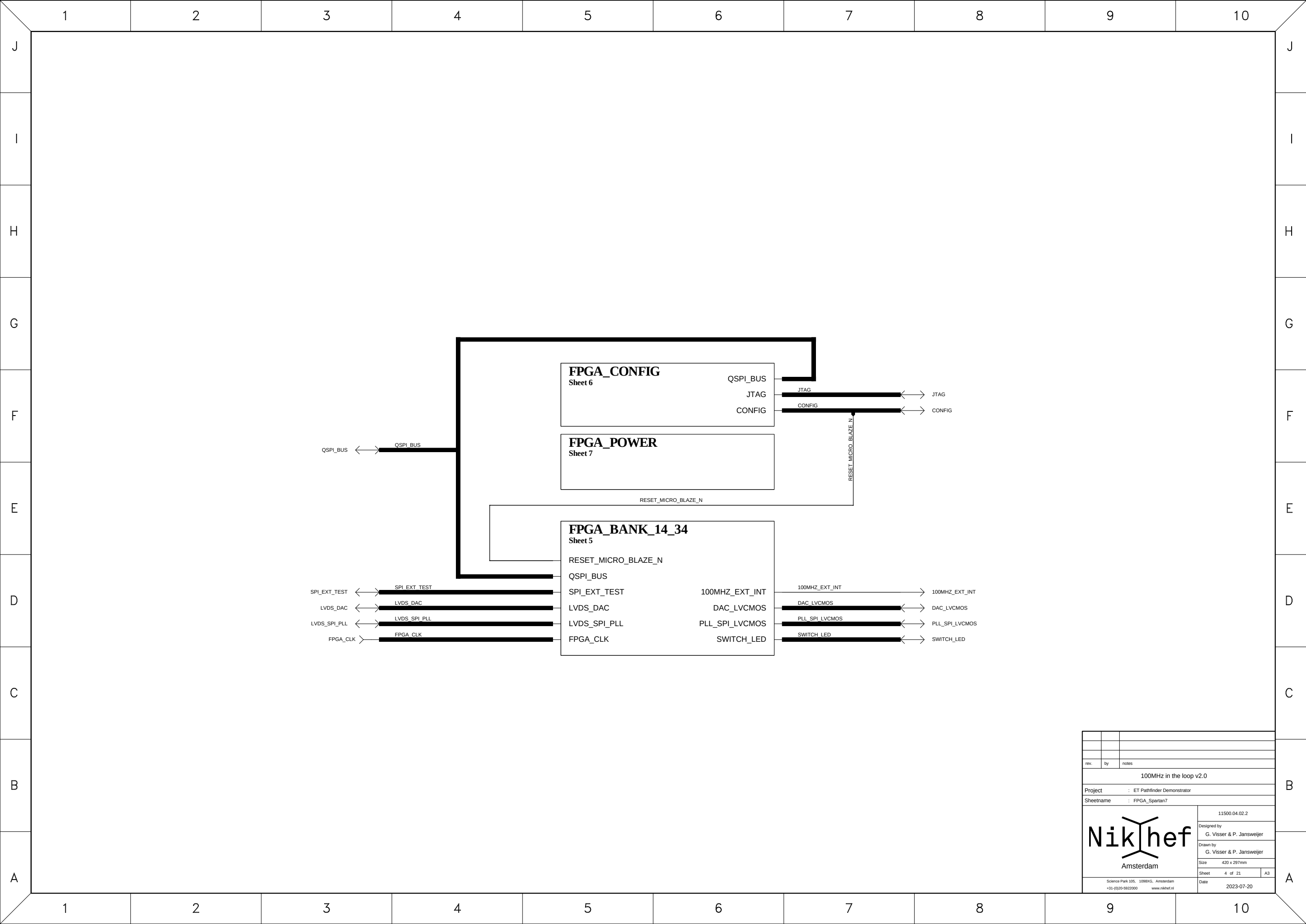


Text on Board =>
LVDS !

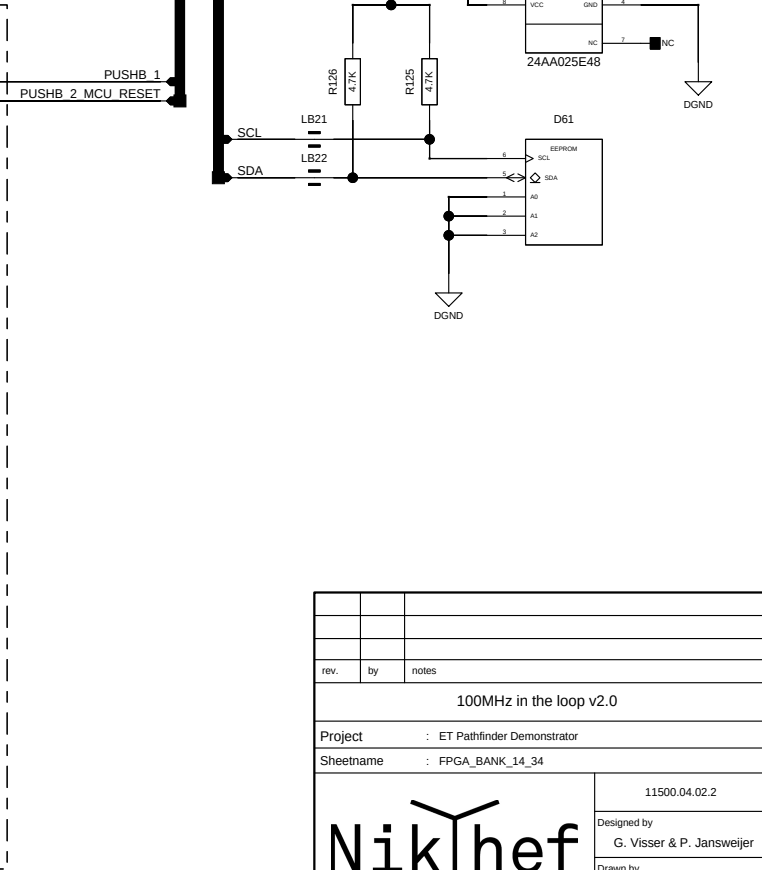
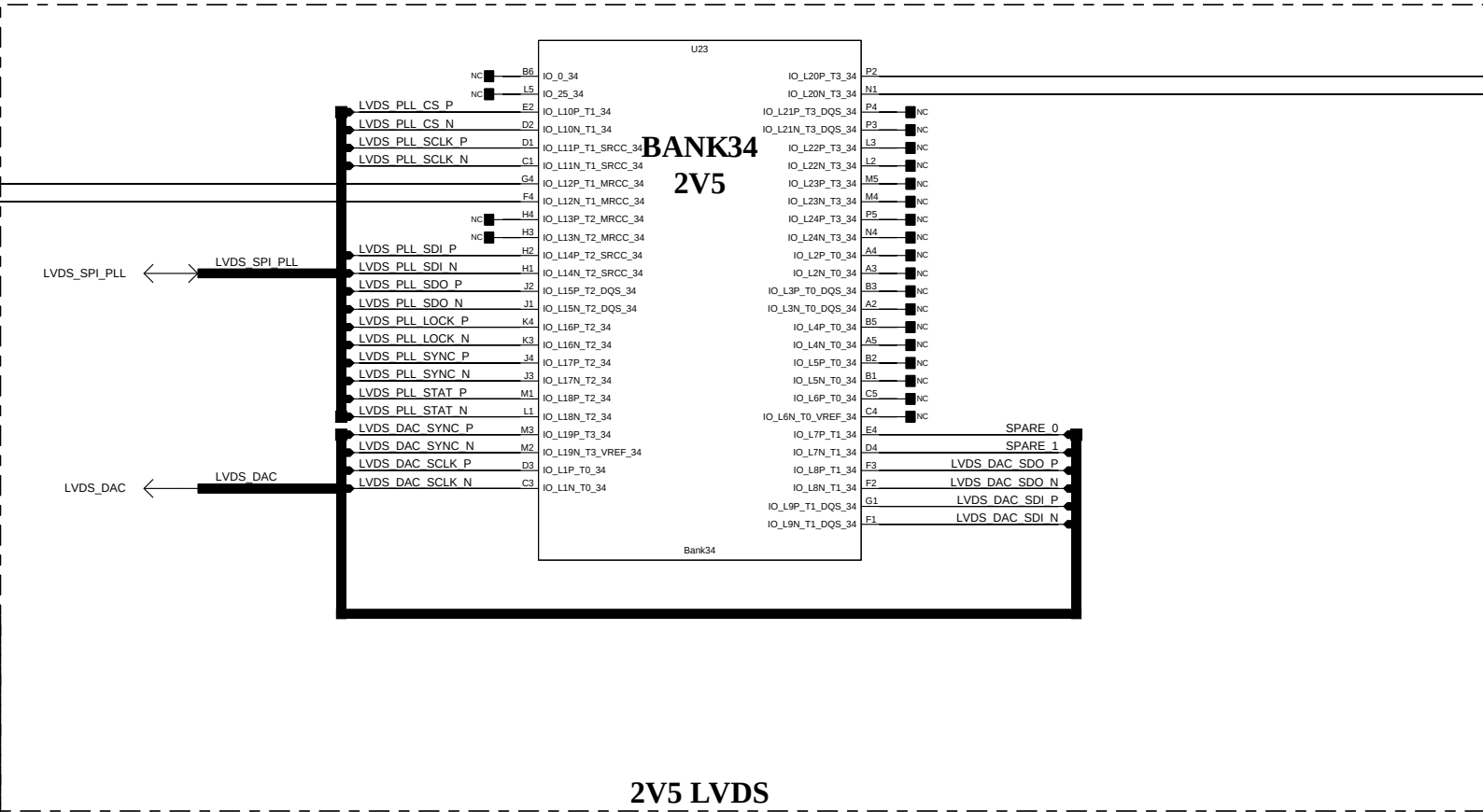
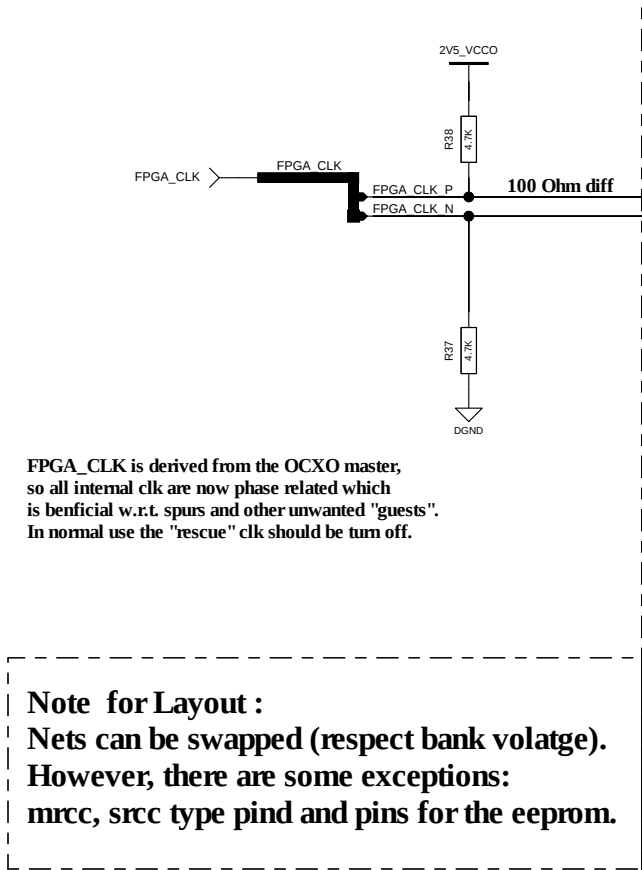
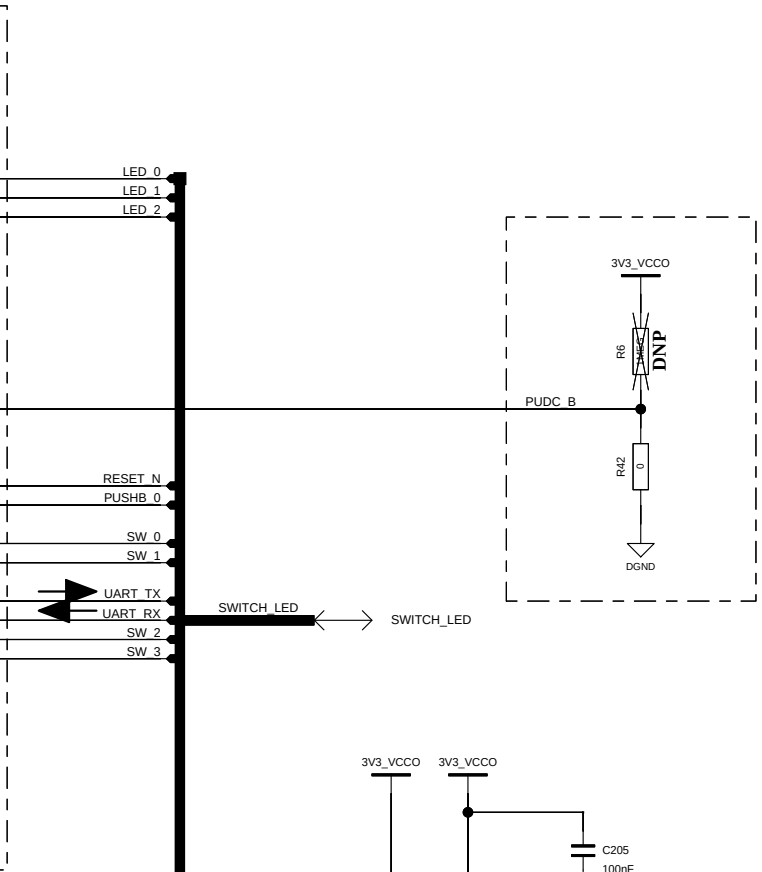
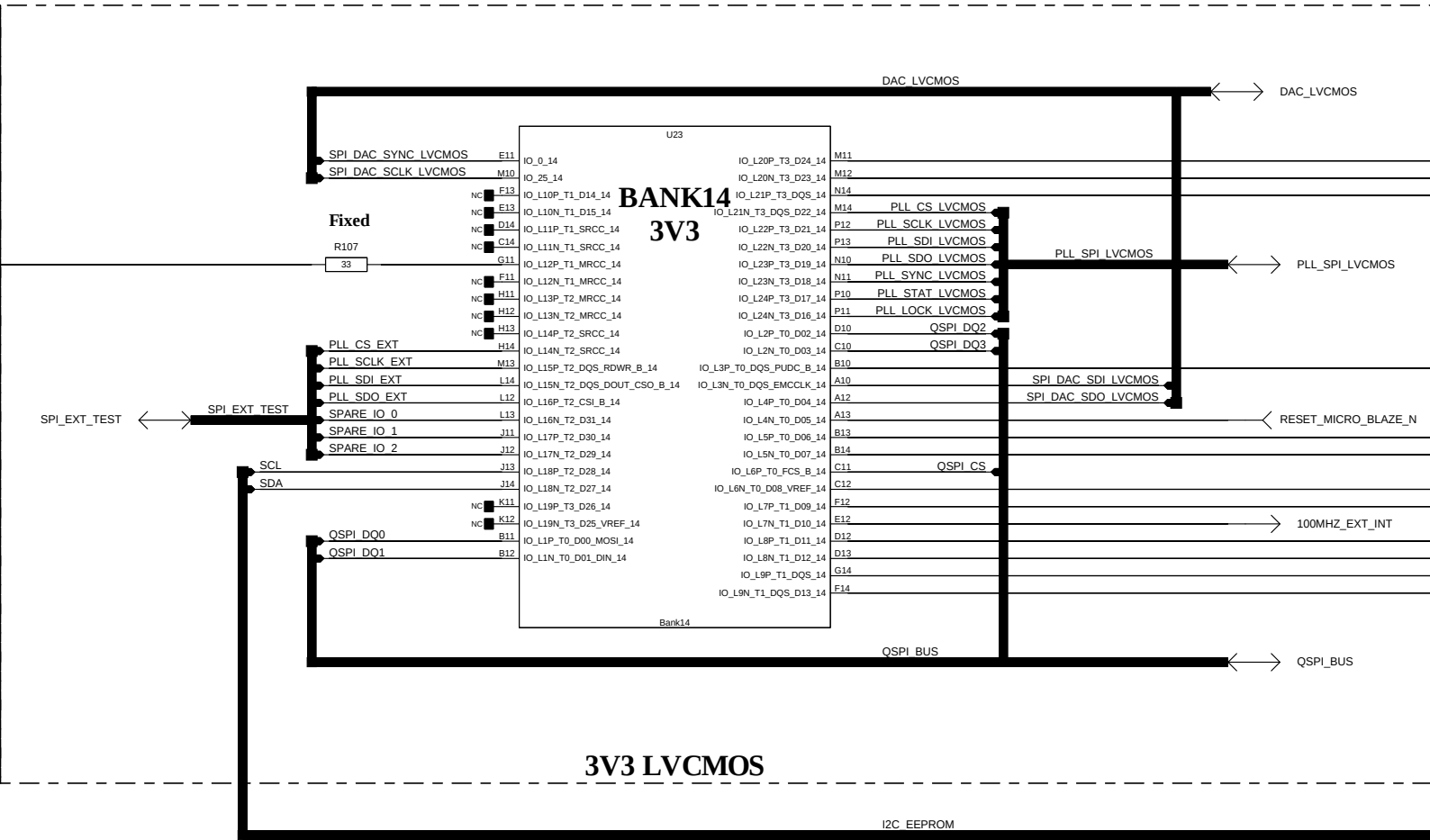
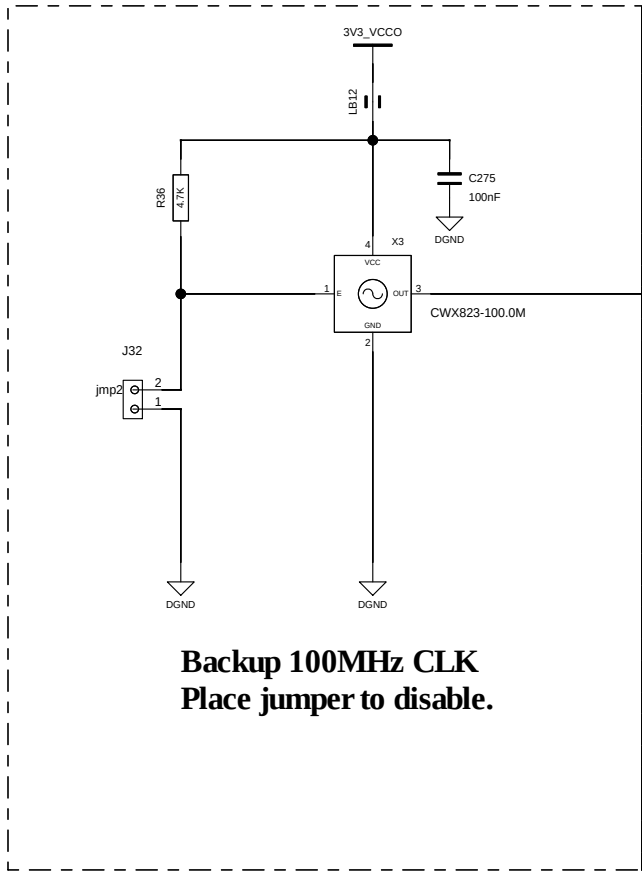
From WR. Tune
Reference oscillator.



rev.	by	notes
100MHz in the loop v2.0		
Project : ET Pathfinder Demonstrator		
Sheetname : Digital_IO		
		11500.04.02.2
		Designed by G. Visser & P. Jansweijer
		Drawn by G. Visser & P. Jansweijer
		Size 420 x 297mm
		Sheet 3 of 21 A3
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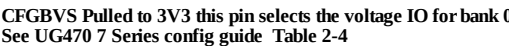


rev.	by	notes
100MHz in the loop v2.0		
Project : ET Pathfinder Demonstrator		
Sheetname : FPGA_Spartan7		
Nikhef Amsterdam		11500.04.02.2
		Designed by G. Visser & P. Jansweijer
		Drawn by G. Visser & P. Jansweijer
		Size 420 x 297mm
		Sheet 4 of 21A3
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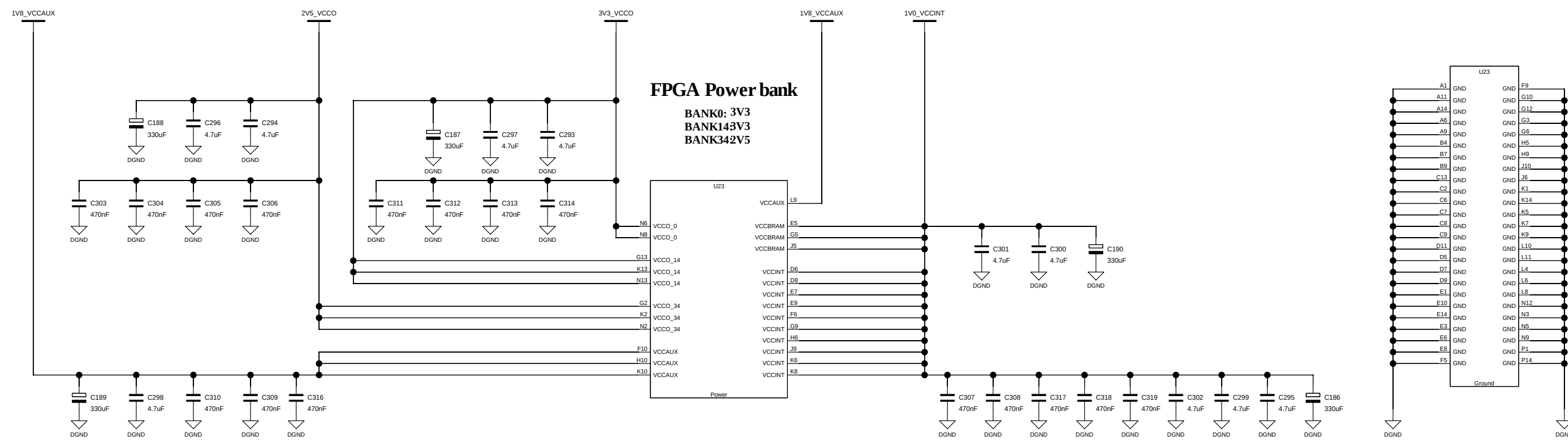
Note for Layout :
Nets can be swapped (respect bank volatge).
However, there are some exceptions:
mrcc, srcc type pind and pins for the eeprom.

rev.	by	notes
100MHz in the loop v2.0		
Project : ET Pathfinder Demonstrator		
Sheetname : FPGA_BANK_14_34		
		11500.04.02.2
		Designed by G. Visser & P. Jansweijer
		Drawn by G. Visser & P. Jansweijer
		Size 420 x 297mm
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Date 2023-07-20		



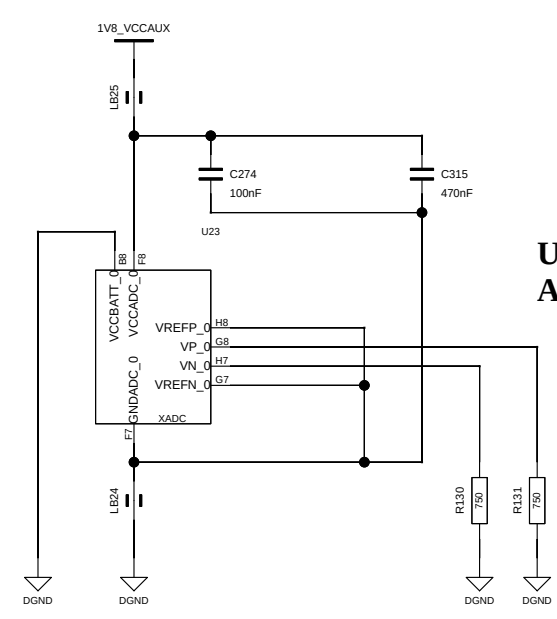
Nikhef
Amsterdam

11500.04.02.2	
Designed by G. Visser & P. Jansweijer	
Drawn by G. Visser & P. Jansweijer	
Size	420 x 297mm
Sheet	6 of 21
Date	2023-07-20



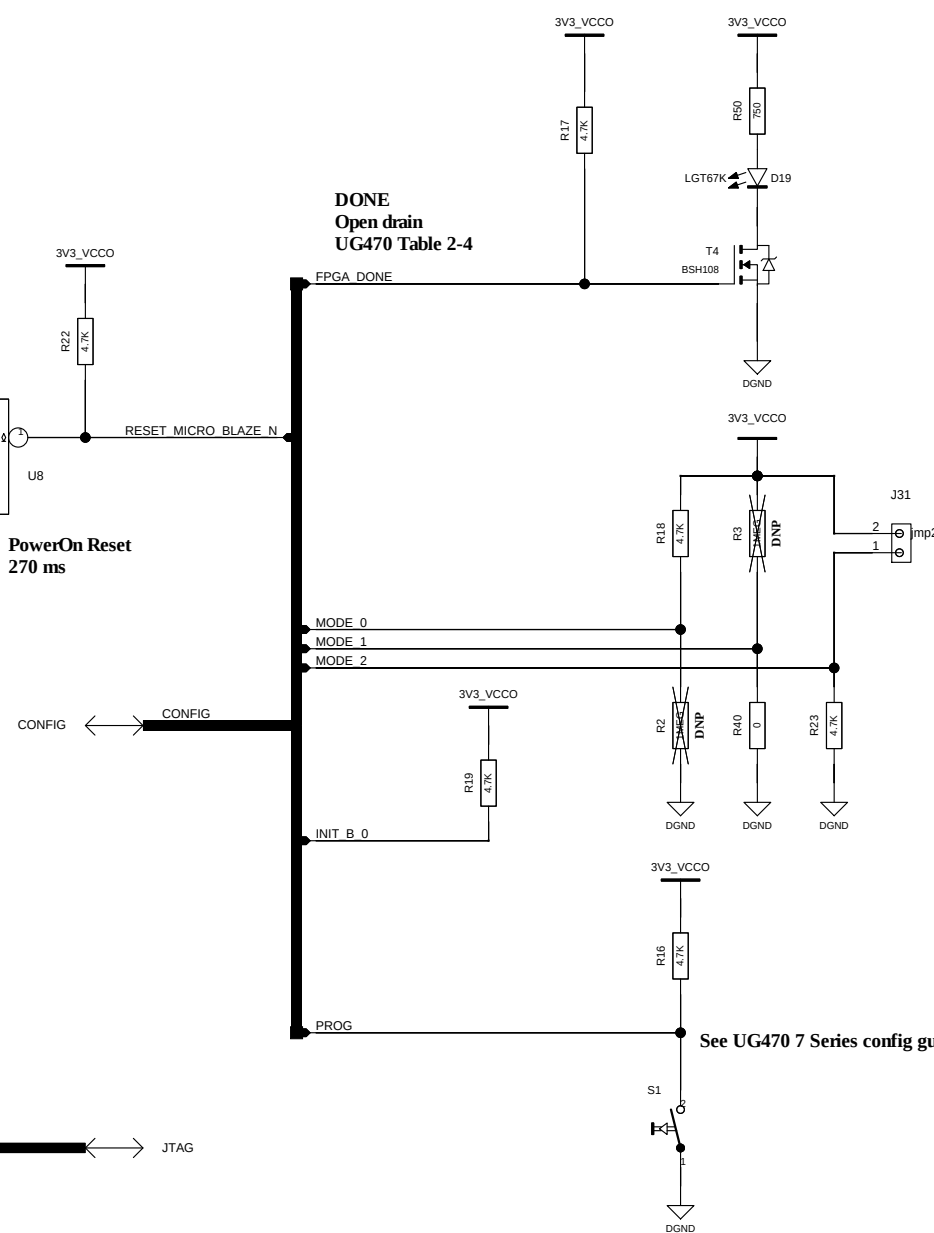
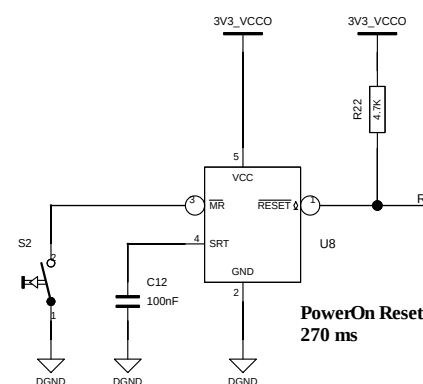
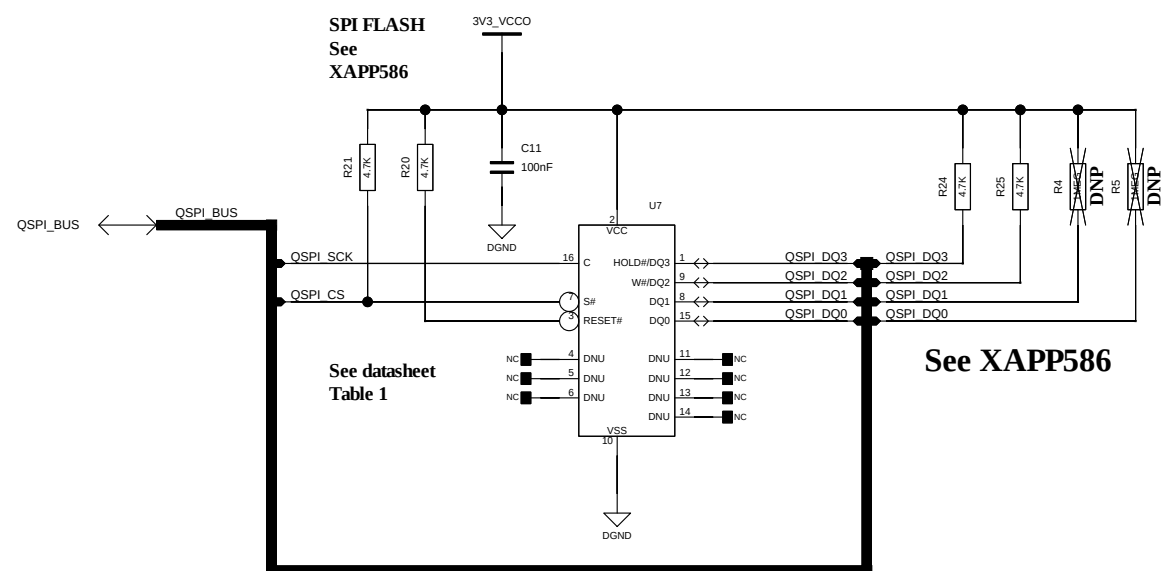
UG483 Table 2-1 (XC7S50 FTGB196):
VCCINT: 1x 100uF, 3x 4.7uF, 5x 0.47uF
VCCBRAM: 1x 100uF, 1x 47uF, 1x 4.7uF, 1x 0.47uF
VCCAUX: 1x 47uF, 1x 4.7uF, 3x 0.47uF
VCCO: 1x 47uF, 2x 4.7uF, 4x 0.47uF

DS189 Table 2 note 9
If battery is not used,
connect VCCBATT to either
ground or VCCAUX

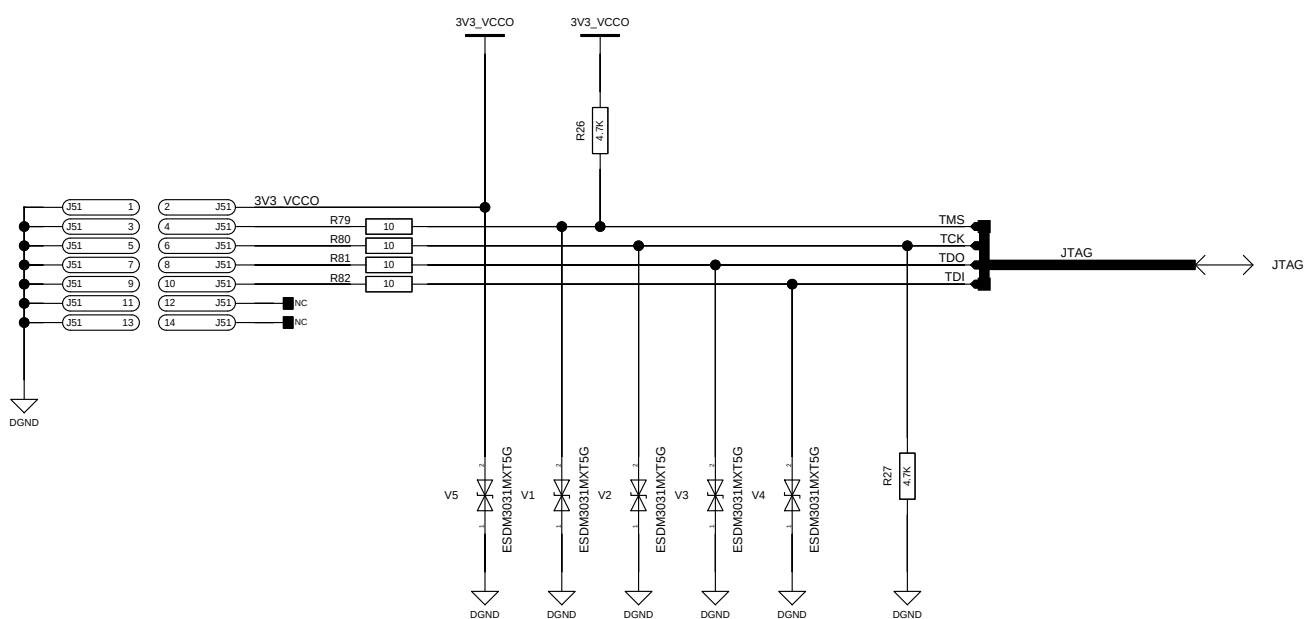


UG480 Figure 1-2
ADC is not used in this desgin

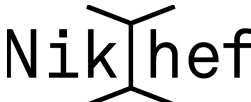
rev.	by	notes
100MHz in the loop v2.0		
Project : ET Pathfinder Demonstrator		
Sheetname : FPGA_POWER		
		11500.04.02.2
		Designed by G. Visser & P. Jansweijer
		Drawn by G. Visser & P. Jansweijer
		Size 420 x 297mm
		Sheet 7 of 21 A3
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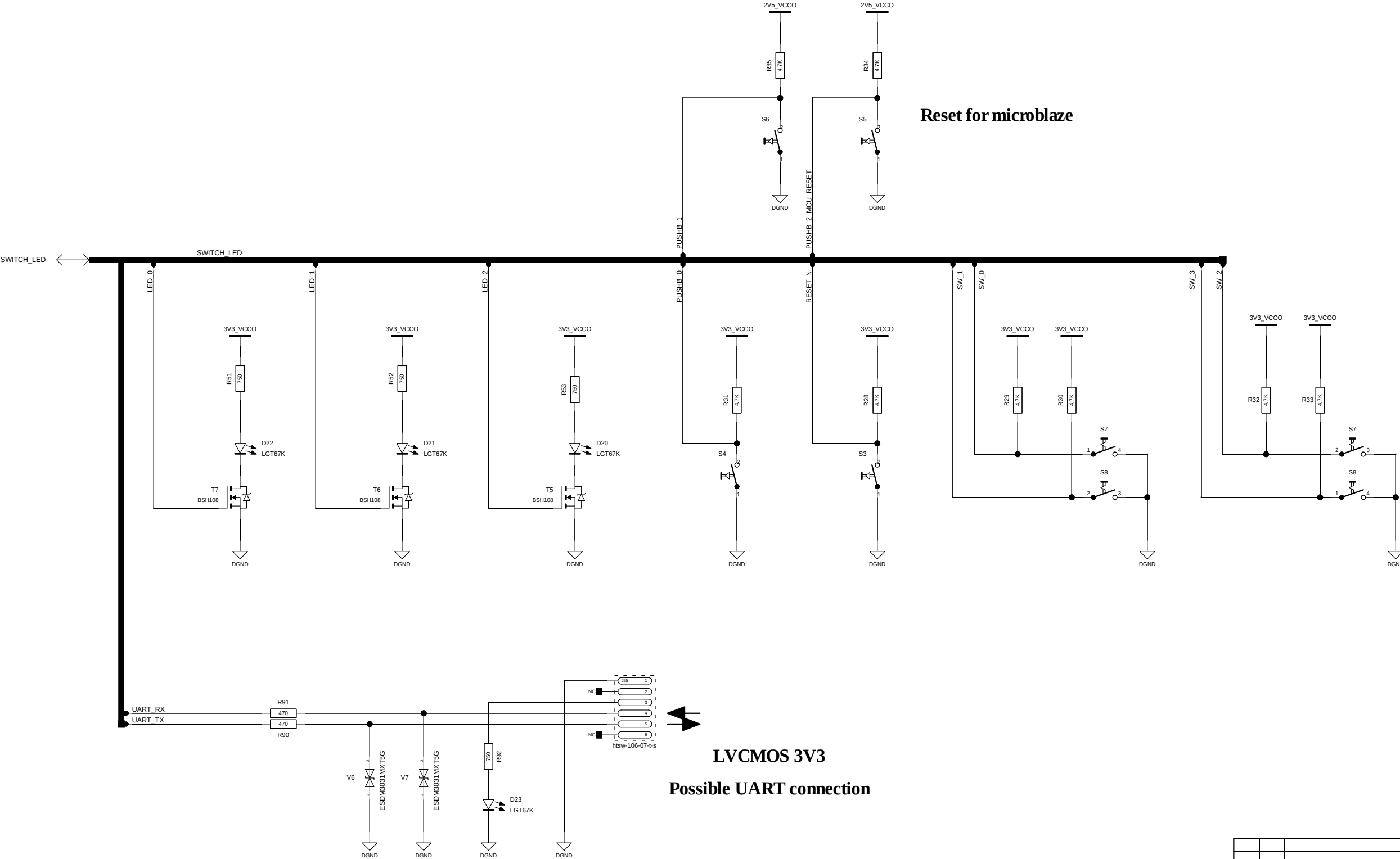
UG470 Table 2-1

Configuration mode	M2	M1	M0	Bush With
Master Serial	0	0	0	x1
Master SPI	0	0	1	x1,x2,x4
Master BPI	0	1	0	x8,x16
	0	1	1	
Master SelectMap	1	0	0	x8,x16
JTAG	1	0	1	x1
Slave SelectMap	1	1	0	x8,x16,x32
Slave Serial	1	1	1	x1

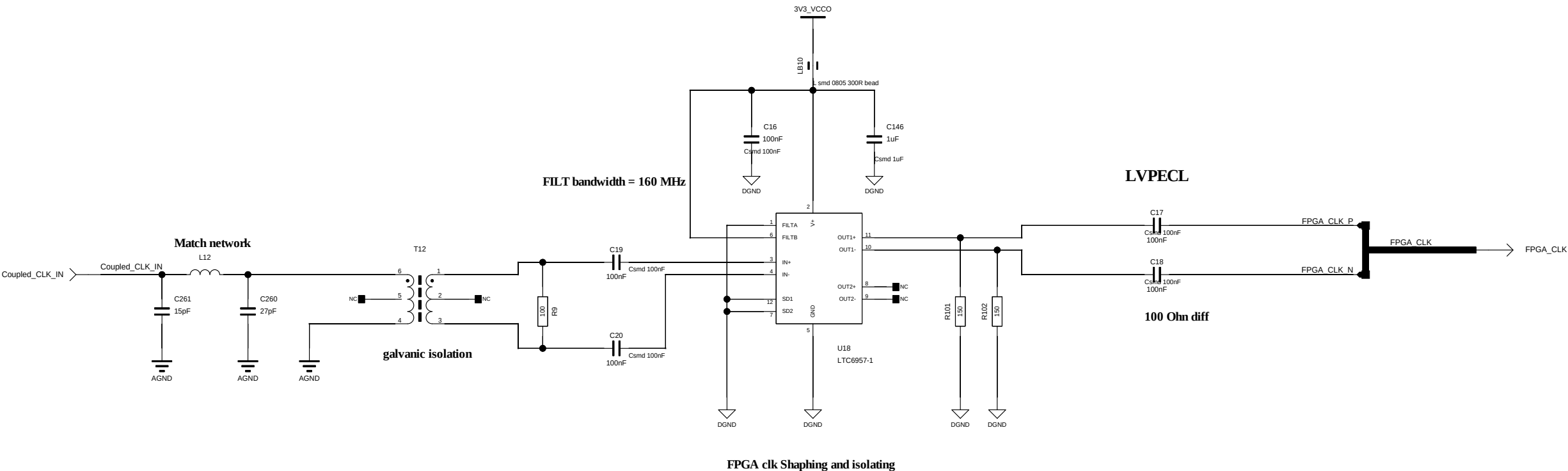


ESD protection

rev.	by	notes	
100MHz in the loop v2.0			
Project : ET Pathfinder Demonstrator			
Sheetname : FPGA_EEPROM_AND_JTAG			
		11500.04.02.2	
		Designed by G. Visser & P. Janszweijer	
		Drawn by G. Visser & P. Janszweijer	
		Size 420 x 297mm	
		Sheet 8 of 21	A
		Date 2023-07-20	
Science Park 105, 1098XG, Amsterdam +31-(0)20-5922000 www.nikhef.nl			

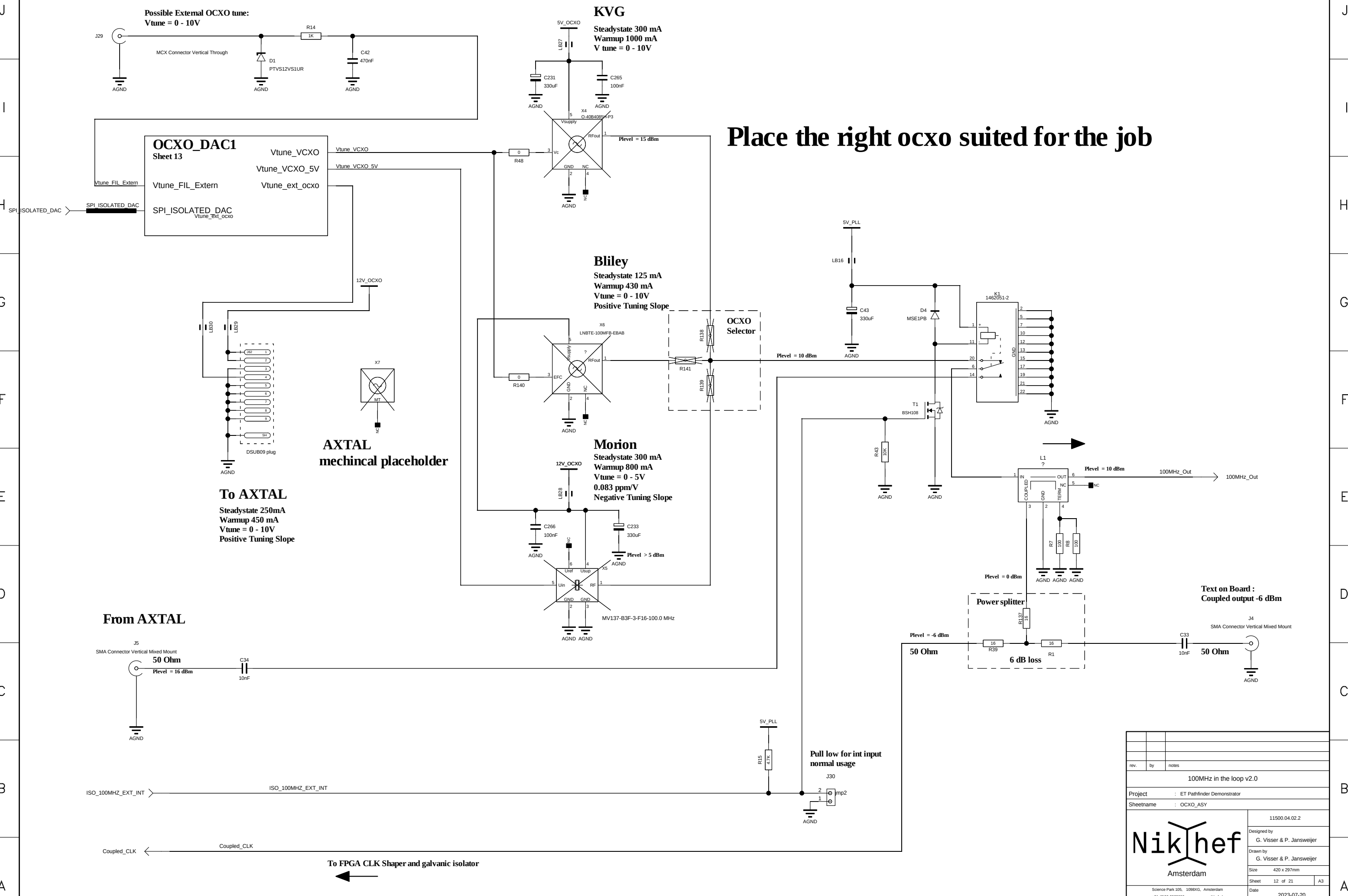


rev.	by	notes
100MHz in the loop v2.0		
Project : ET Pathfinder Demonstrator		
Sheetname : Switch_and_led		
		11500.04.02.2
		Designed by G. Visser & P. Jansweijer
		Drawn by G. Visser & P. Jansweijer
		Size 420 x 297mm
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		Date 2023-07-20



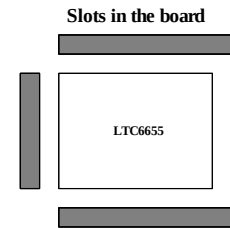
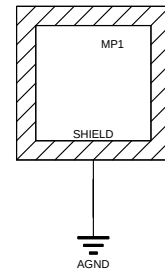
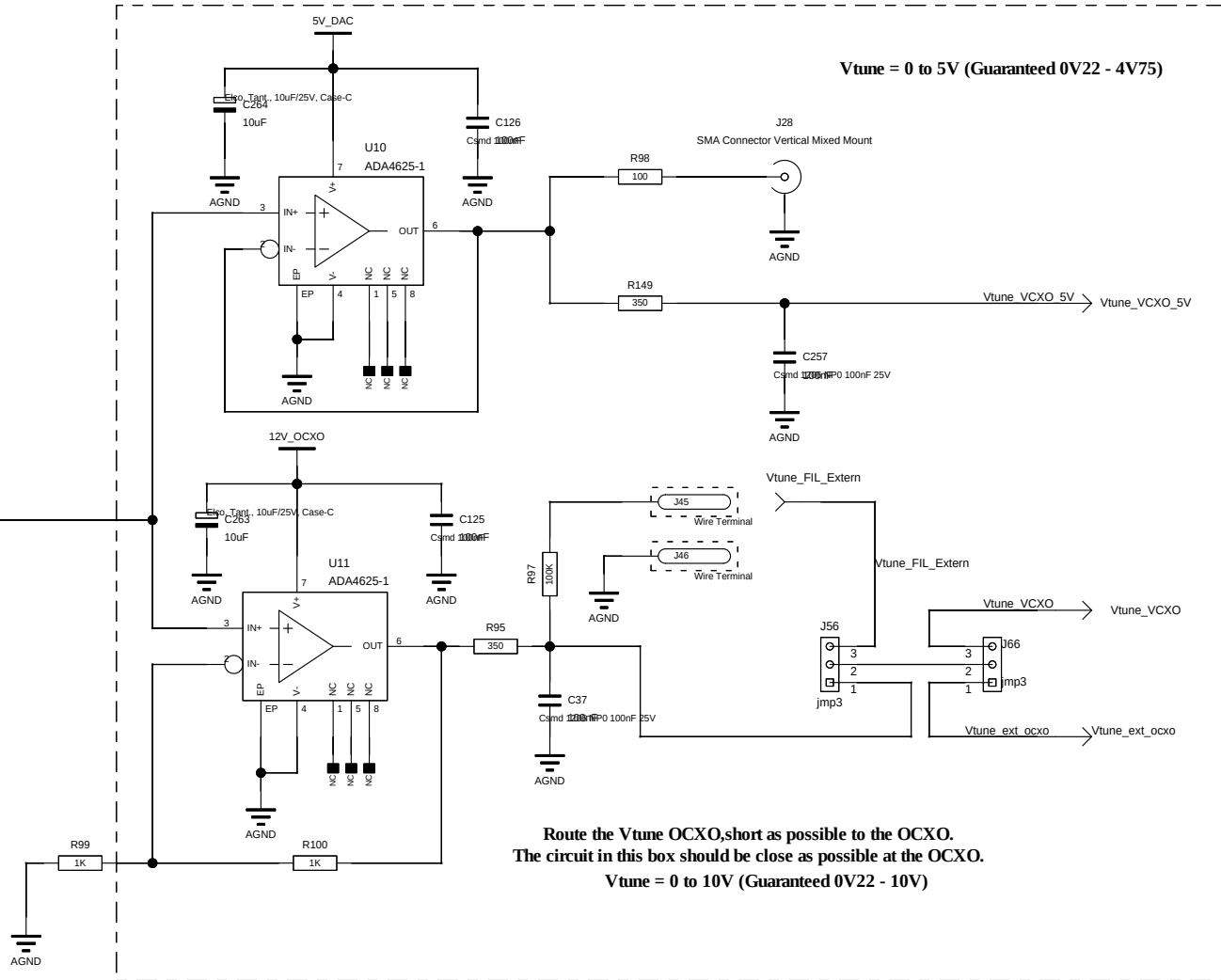
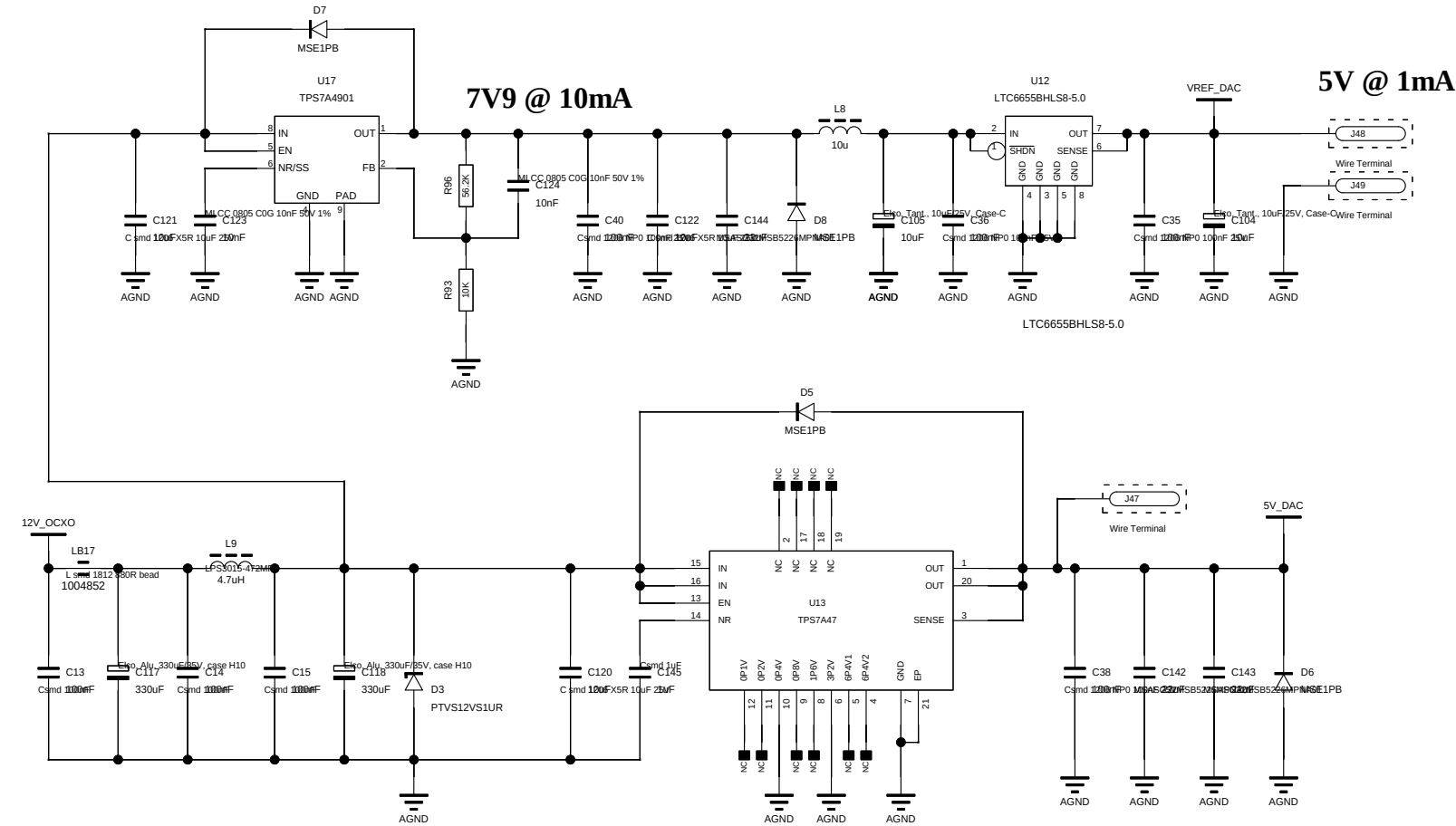
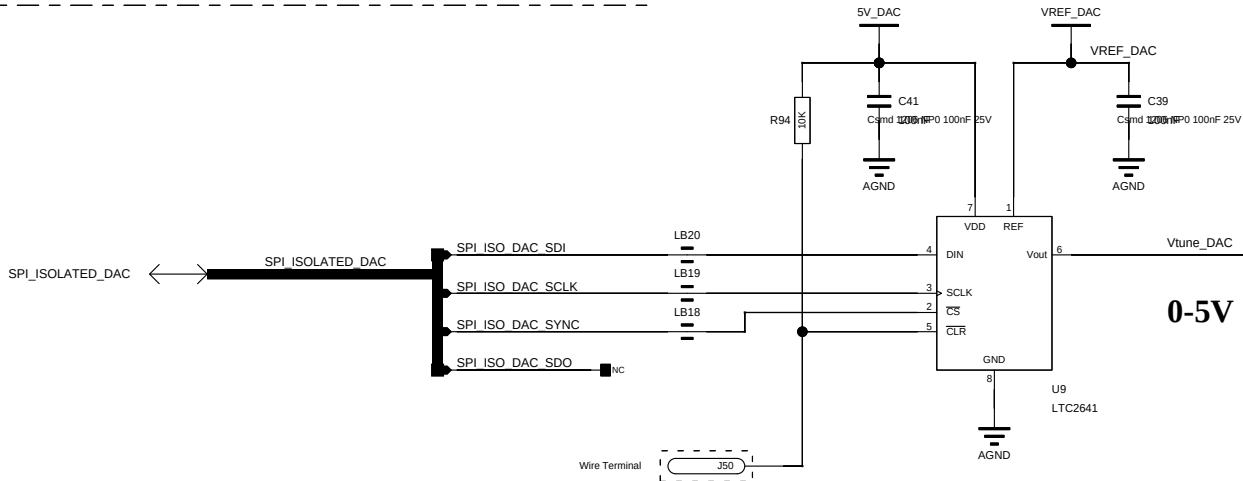
rev.	by	notes
100MHz in the loop v2.0		
Project : ET Pathfinder Demonstrator		
Sheetname : CLK_SHAPER		
		11500.04.02.2
		Designed by G. Visser & P. Jansweijer
		Drawn by G. Visser & P. Jansweijer
		Size 420 x 297mm
		Sheet 11 of 21 A3
Science Park 105, 1098XG, Amsterdam +31-(0)20-5922000 www.nikhef.nl		Date 2023-07-20

Place the right ocxo suited for the job

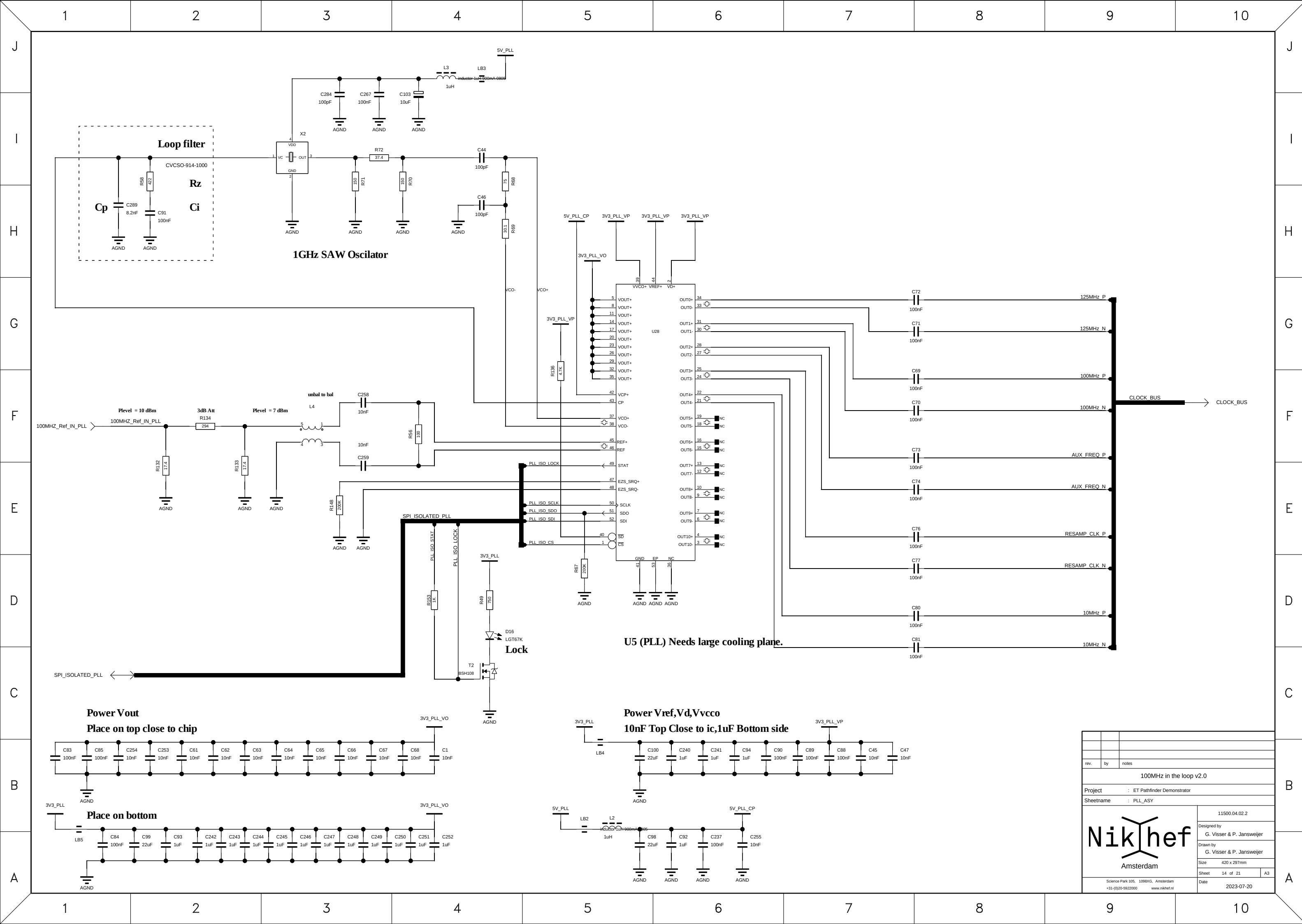


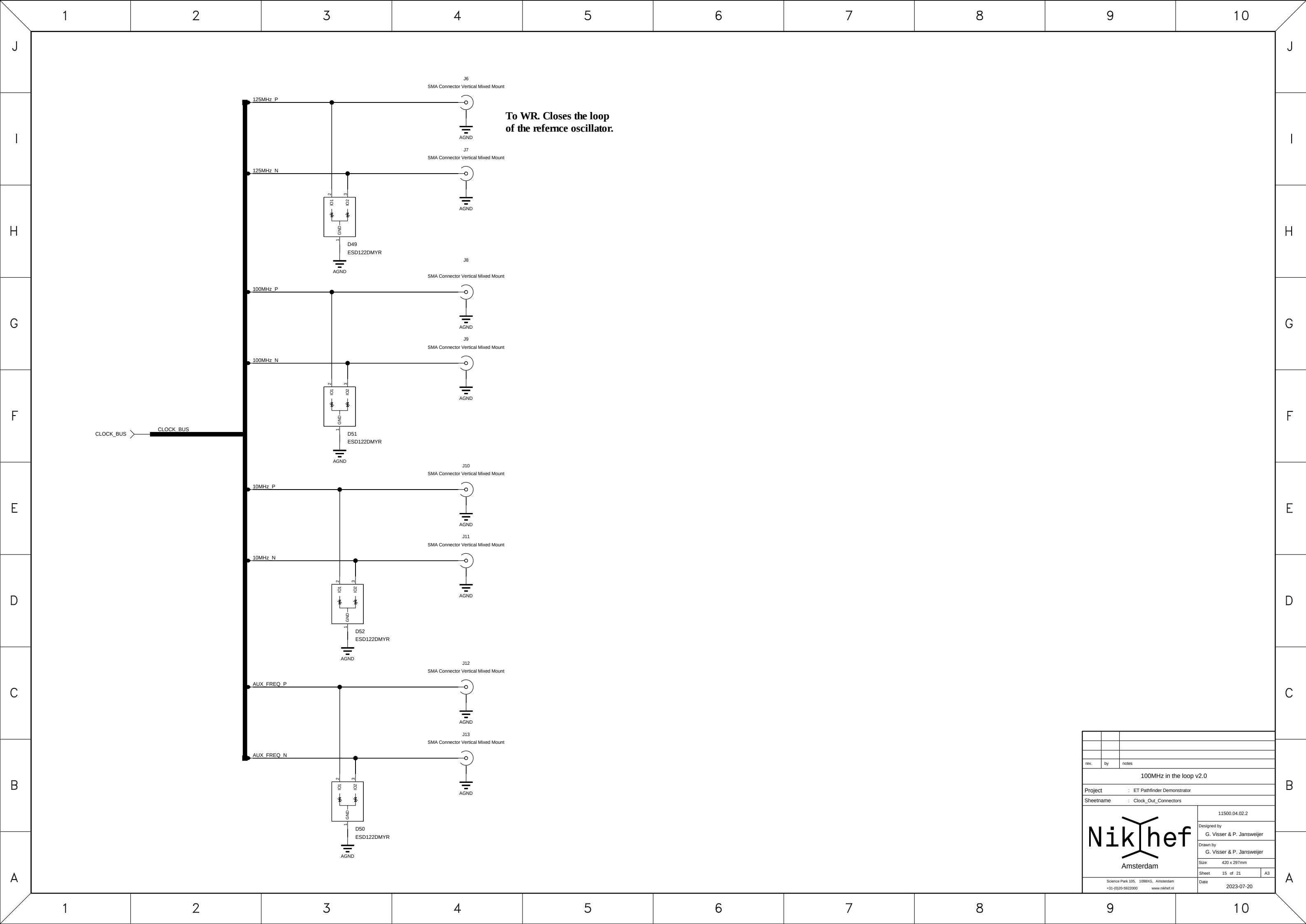
rev.	by	notes
100MHz in the loop v2.0		
Project : ET Pathfinder Demonstrator		
Sheetname : OCXO_ASY		
Nikhef Amsterdam		11500.04.02.2
		Designed by G. Visser & P. Jansweijer
		Drawn by G. Visser & P. Jansweijer
		Size 420 x 297mm
		Sheet 12 of 21 A3
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Place all componest under the shielded can, to shield it from EMI, and reduce the airflow around this circuit



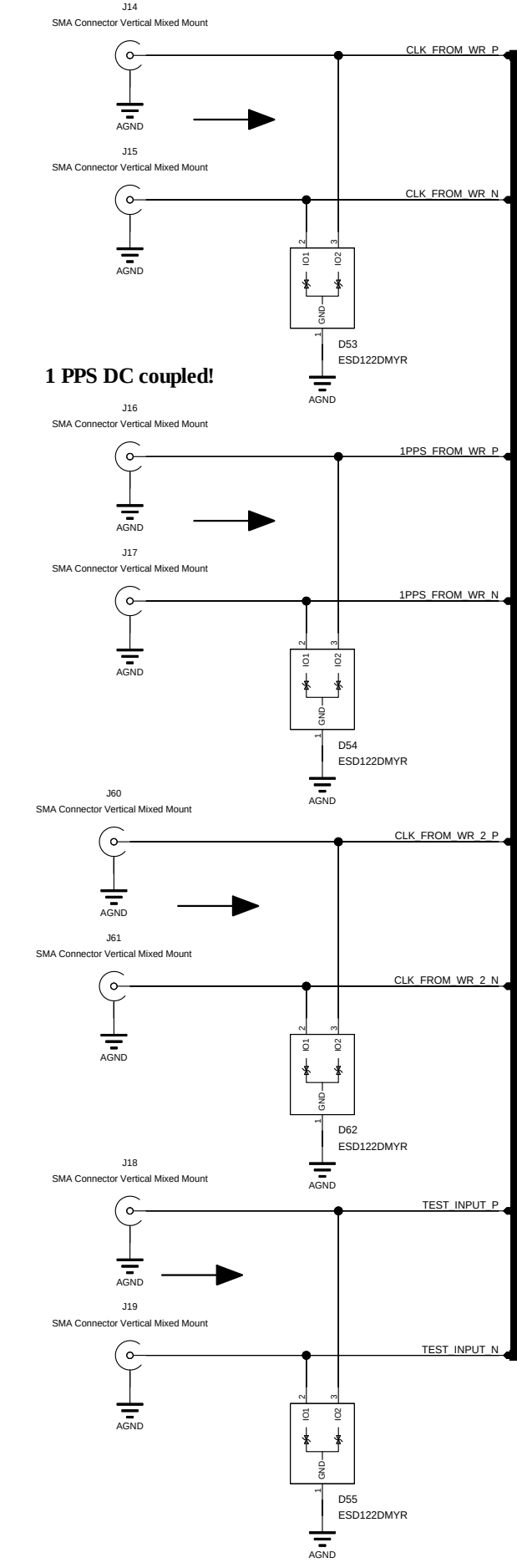
rev.	by	notes
100MHz in the loop v2.0		
Project : ET Pathfinder Demonstrator		
Sheetname : OCXO_DAC		
Nikhef Amsterdam		11500.04.02.2
		Designed by G. Visser & P. Jansweijer
		Drawn by G. Visser & P. Jansweijer
		Size 420 x 297mm
		Sheet 13 of 21 A3
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rev.	by	notes
100MHz in the loop v2.0		
Project : ET Pathfinder Demonstrator		
Sheetname : Clock_Out_Connectors		
		11500.04.02.2
		Designed by G. Visser & P. Jansweijer
		Drawn by G. Visser & P. Jansweijer
		Size 420 x 297mm
		Sheet 15 of 21A3
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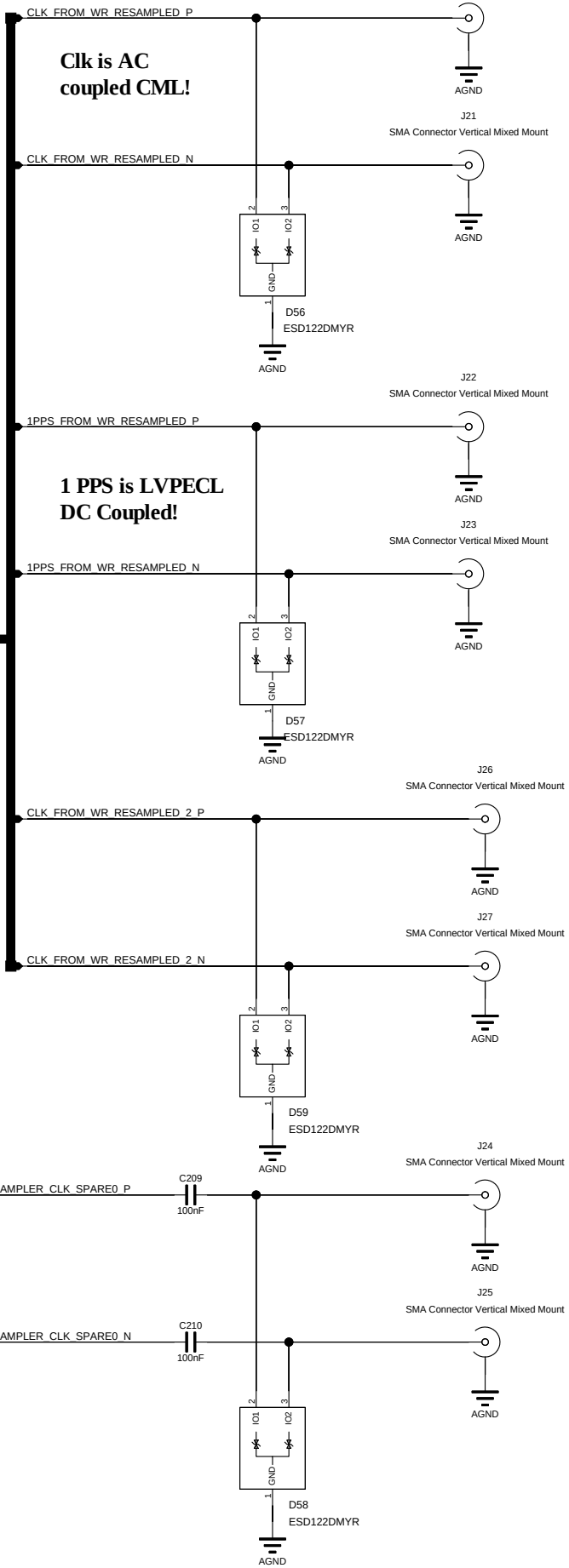
CLOCKS From WR
Phase aligned with WR
125 MHz reference clock.



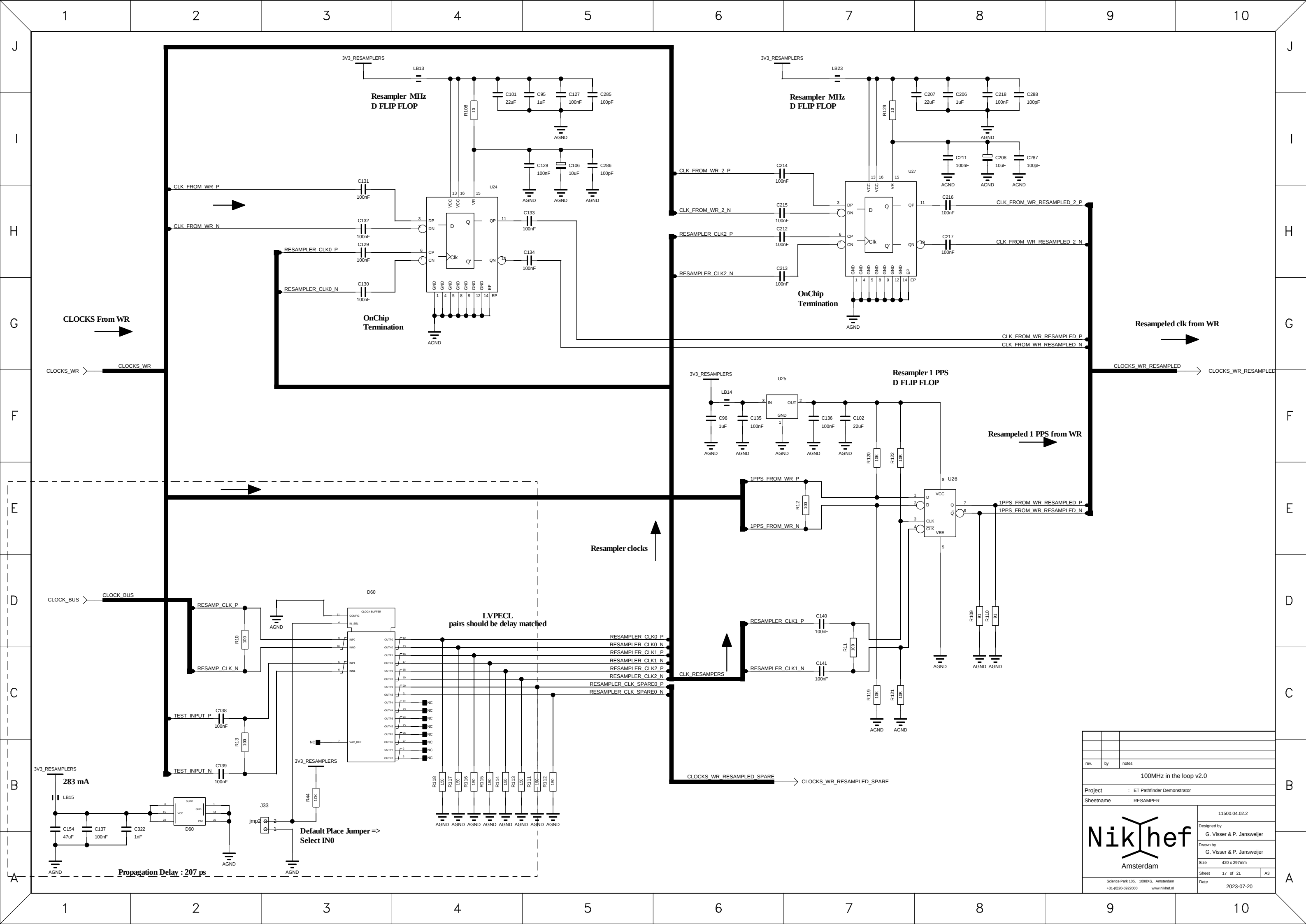
Resampler
Sheet 17

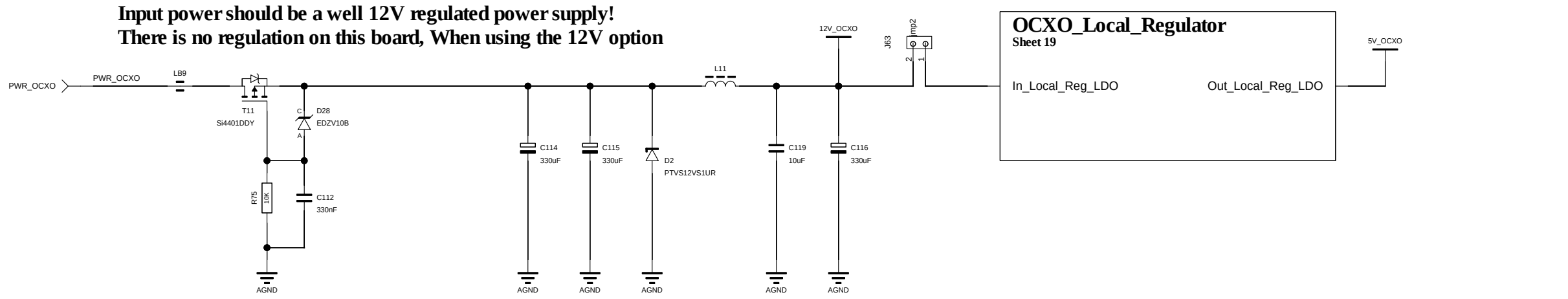
CLOCKS_WR CLOCKS_WR_RESAMPLED
CLOCK_BUS CLOCK_BUS
CLOCKS_WR_RESAMPLED_SPARE

Resampled Clk and
1 PPS from WR



rev.	by	notes
100MHz in the loop v2.0		
Project : ET Pathfinder Demonstrator		
Sheetname : WR_CLOCKS_IO		
		11500.04.02.2
		Designed by G. Visser & P. Jansweijer
		Drawn by G. Visser & P. Jansweijer
		Size 420 x 297mm
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		Date 2023-07-20





OCXO_Local_Regulator
Sheet 19

In_Local_Reg_LDO

Out_Local_Reg_LDO



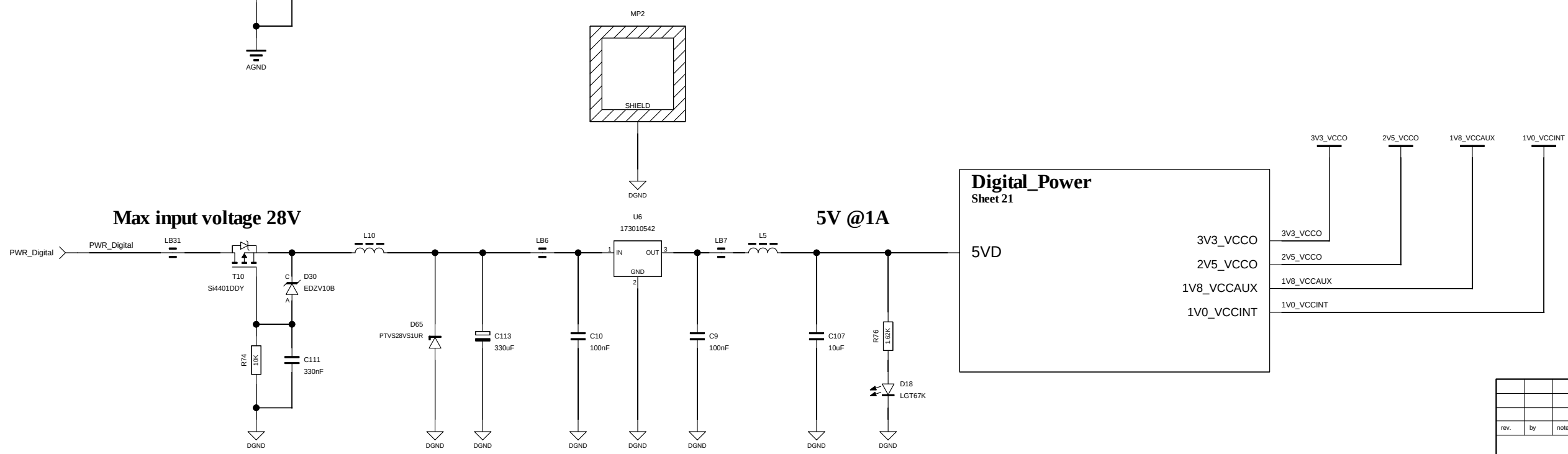
Power_Analog
Sheet 20

PWR_Vanalog_Prot

5V_PLL

3V3_PLL

3V3_RESAMPLERS



Digital_Power
Sheet 21

5VD

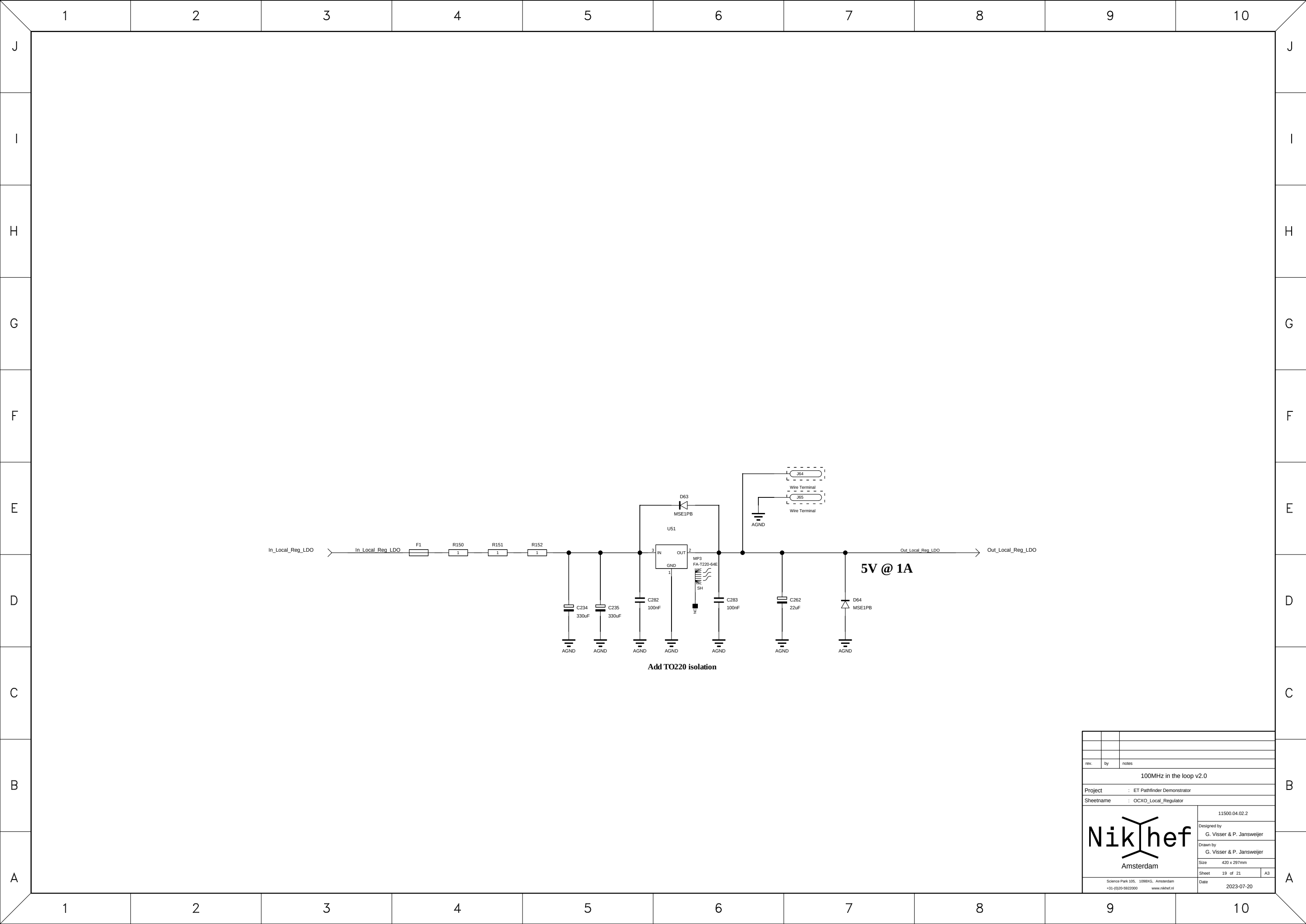
3V3_VCCO

2V5_VCCO

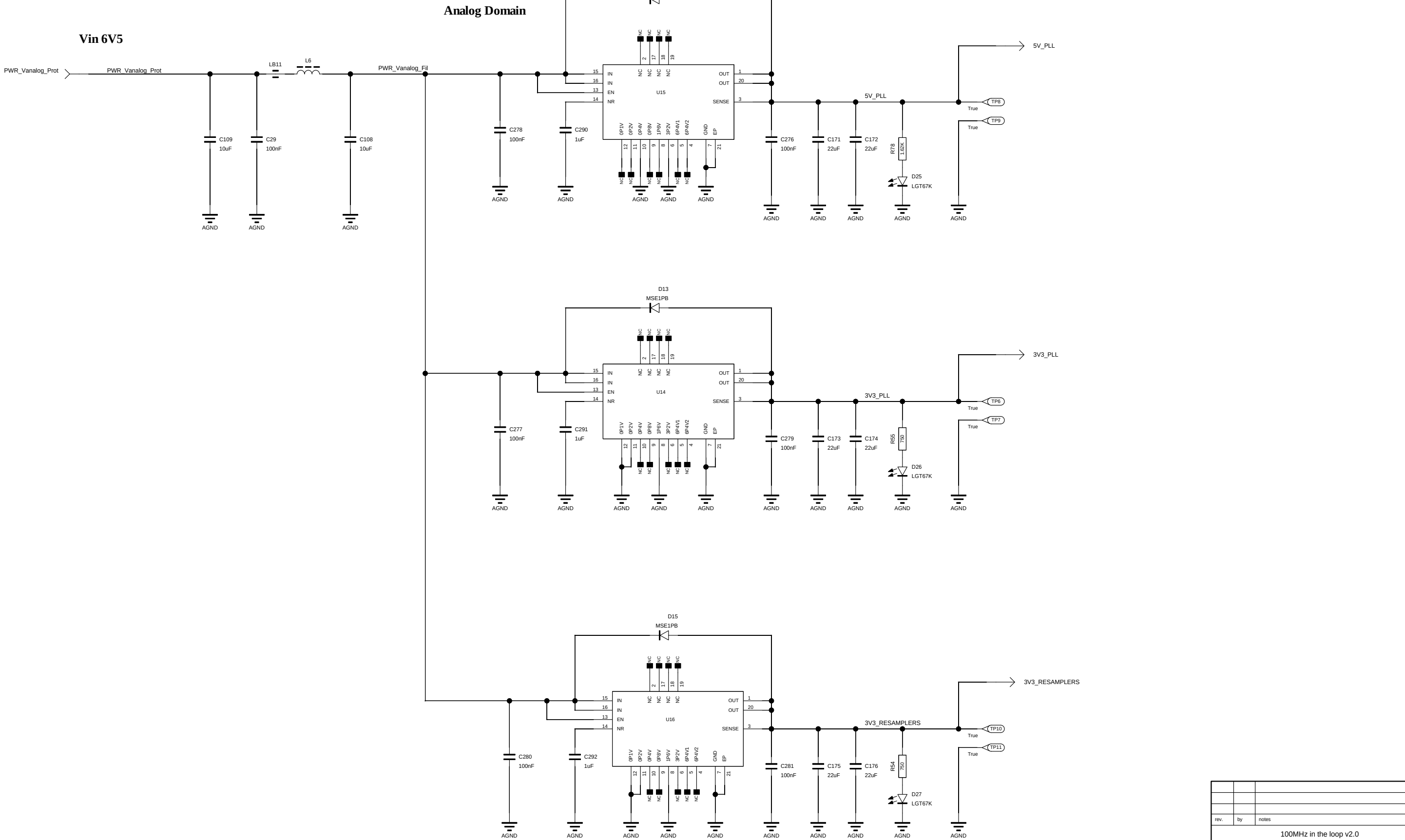
1V8_VCCAUX

1V0_VCCINT

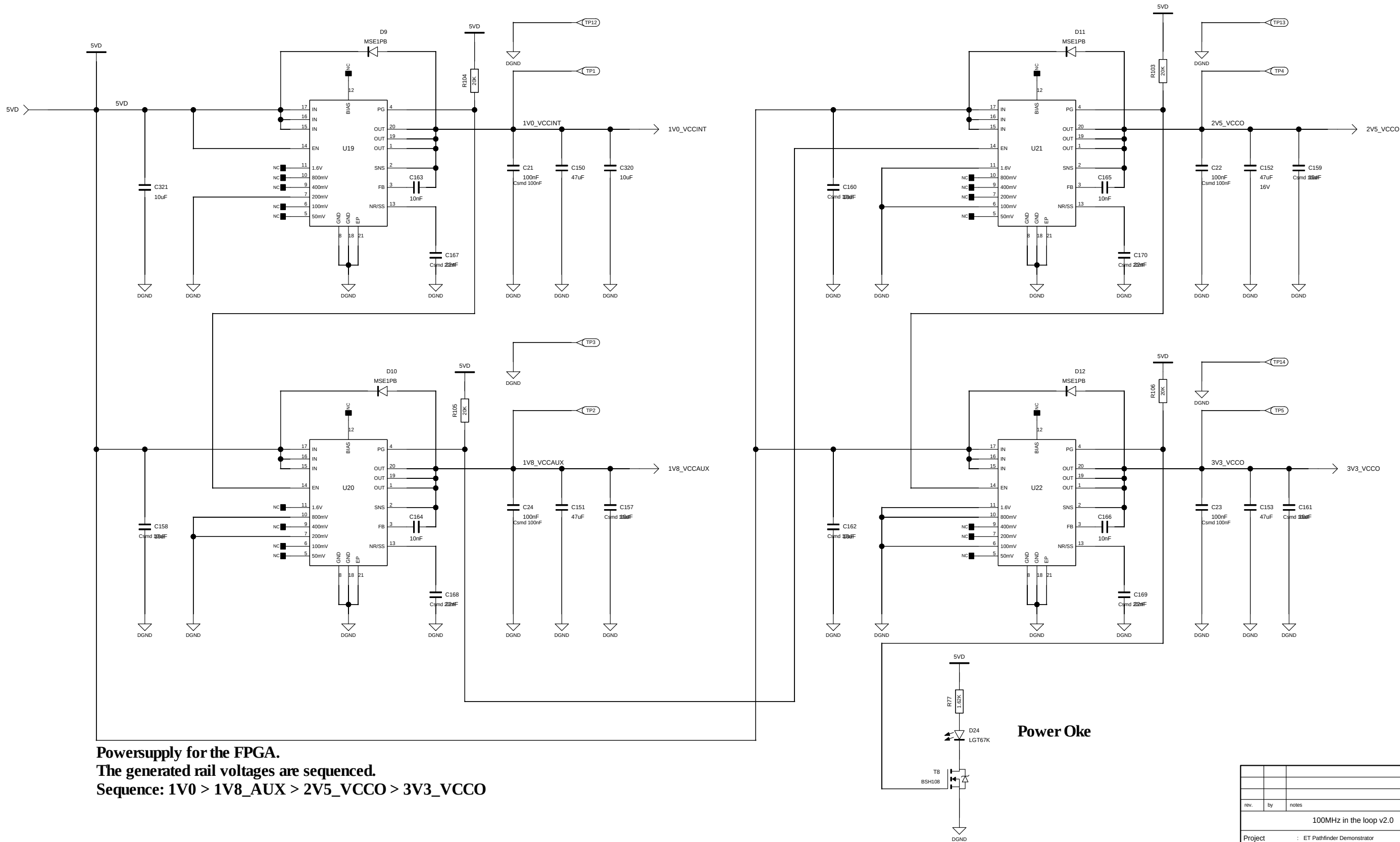
rev.	by	notes
100MHz in the loop v2.0		
Project : ET Pathfinder Demonstrator		
Sheetname : Power		
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		Designed by G. Visser & P. Jansweijer
		Drawn by G. Visser & P. Jansweijer
		Size 420 x 297mm
		Sheet 18 of 21 A3
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rev.	by	notes
100MHz in the loop v2.0		
Project : ET Pathfinder Demonstrator		
Sheetname : OCXO_Local_Regulator		
		11500.04.02.2
		Designed by G. Visser & P. Jansweijer
		Drawn by G. Visser & P. Jansweijer
		Size 420 x 297mm
		Sheet 19 of 21 A3
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rev.	by	notes
100MHz in the loop v2.0		
Project : ET Pathfinder Demonstrator		
Sheetname : Power_Analog		
		11500.04.02.2
		Designed by G. Visser & P. Jansweijer
		Drawn by G. Visser & P. Jansweijer
		Size 420 x 297mm
		Sheet 20 of 21 A3
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Powersupply for the FPGA.
The generated rail voltages are sequenced.
Sequence: 1V0 > 1V8_AUX > 2V5_VCCO > 3V3_VCCO

rev.	by	notes
100MHz in the loop v2.0		
Project : ET Pathfinder Demonstrator		
Sheetname : Digital_Power		
		11500.04.02.2
		Designed by G. Visser & P. Jansweijer
		Drawn by G. Visser & P. Jansweijer
		Size 420 x 297mm
Science Park 105, 1098XG, Amsterdam +31-(0)20-5922000 www.nikhef.nl		Sheet 21 of 21
		Date 2023-07-20