# Some Phase noise Measurements on FPGA's

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# Contents

# Revision History

| Revision | Date | Author(s) | Description |
|---|---|---|---|
| 0.0 | 20-06-2018 | G C Visser | Created. |

# 1 Introduction

This rapport presents phase noise measurements on FPGA's when used as frequency divider and as buffers

## 1.1 Overview of the measurement system.

As phase noise analyzer a Rohde & Schwarz phase the FSWP, and as source the HP8663a. The source exhibit low phase noise. To fuhrer improve the close in phase noise the generator is locked to a very low noise phase noise OCXO the 8663 from oscilloquartz.The output of the source is converted to a LVDS/CML logic level with the aid of a limiting amplifier. All the measurements of the source are directly made via the liming amplifier.

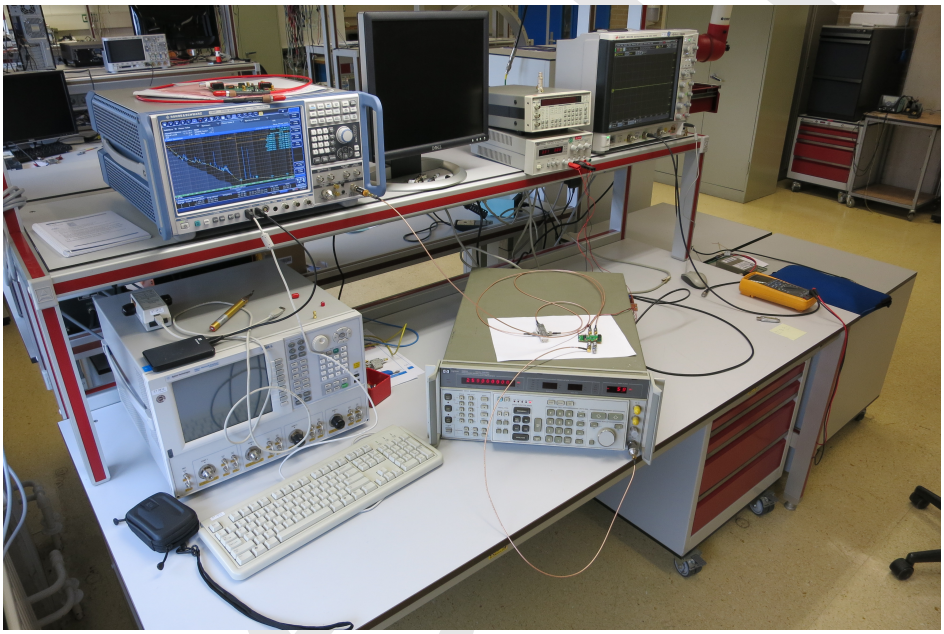

Figure 1: Photograph of the measurement setup

In the following figure 1 is the measurement setup shown, FPGA board and reference OCXO are not shown.

# 2 Measurement results

In the following sub chapters are the measurement results shown.The correlation factor of the phase noise analyzer was set to 100 times 100 correlation gives enough margin to reduce the noise floor of the instrument well below the measured phase nois is.The offset range is set in must cases from 1$HZ$ to 10M$MHz$ Also the is the jitter calculated with the aid of a Matlab script.

## 2.1 Phase noise of the source

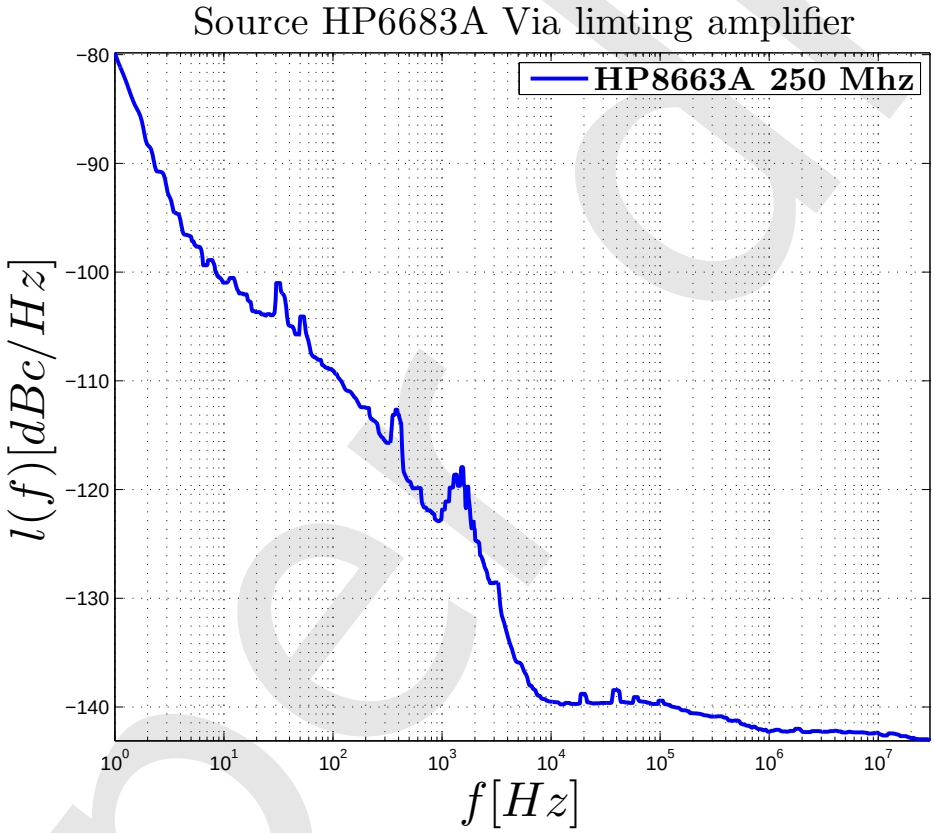


Figure 2: Phase noise of the source via limiting amplifier.

In figure 2 is the total measured phase noise shown of the source including the limiting amplifier.

| Item | Jitter $[ps]$ | Integration range |
|---|---|---|
| HP86683A | 0,242 | 1 to 10e6 $Hz$ |
| HP86683A | 0,207 | 10e3 to 10e6 $Hz$ |

Table 2: Jitter of the source

## 2.2 Kintex series 7

For this test we have used the xilinx kc705 elevation board.

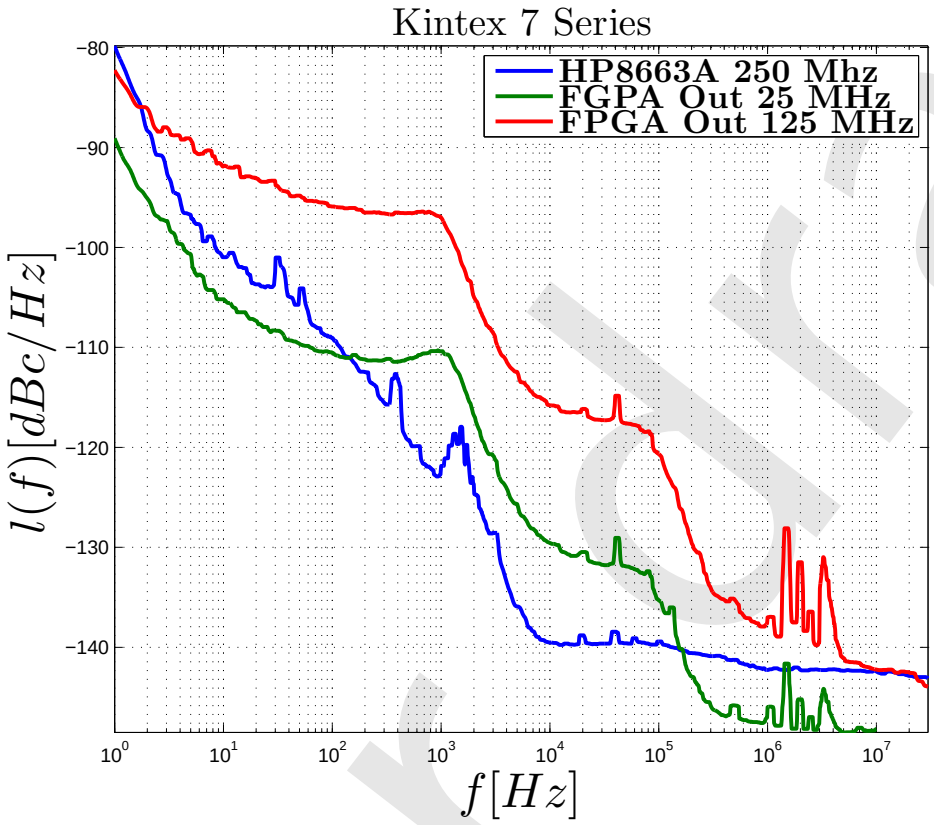


Figure 3: Phase noise dividers made in the kintex series 7 fpga.

| Item | Jitter $[ps]$ | Integration range |
|---|---|---|
| kintex divided by 2 | 1,584 | 1 to 10e6 $Hz$ |
| kintex divided by 2 | 0,718 | 10 to 10e6 $Hz$ |
| kintex divided by 10 | 1,996 | 1 to 10e6 $Hz$ |
| kintex divided by 10 | 1,102 | 10 to 10e6 $Hz$ |

Table 3: Calculated jitter from the phase noise, kintex series 7 FPGA

## 2.3 Purpose built ZYQN™

To measure the additive phase noise to a certain degree an purpose was built see photo 4.The fpga (ZYQN) is powered via low noise LDO's.As first the additive phase noise is measured of a clock input (MGTREF CLK) routed via the fabric to a clock capable output. and as next test the FPGA is loaded with CRC generator to simulate working logic.The logic is clocked from the same source manly the MGTREF CLK.The frequency of the clock is 125MHz.

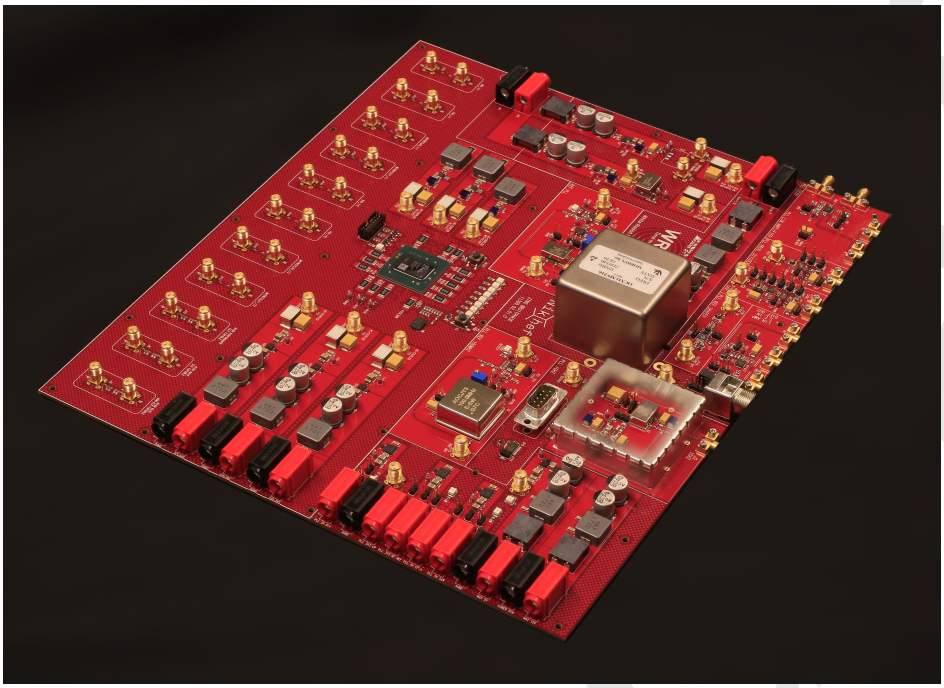

Figure 4: Purpose built FPGA test board ZQYN 7035.

As can been seen in the block schematic 5 there is a in series with the analyzer and the FPGA a limiting amplifier.This is necessary to convert a sine-wave to as square. A sine-wave direct on a "logic" gives a enroumes amount of input chatter due the limiting rise-time of a sine-wave. The used limiting amplifier gives neglecting amount of additional phase noise see for the additive phase noise of used limiting amplfier figure 8 in section 3

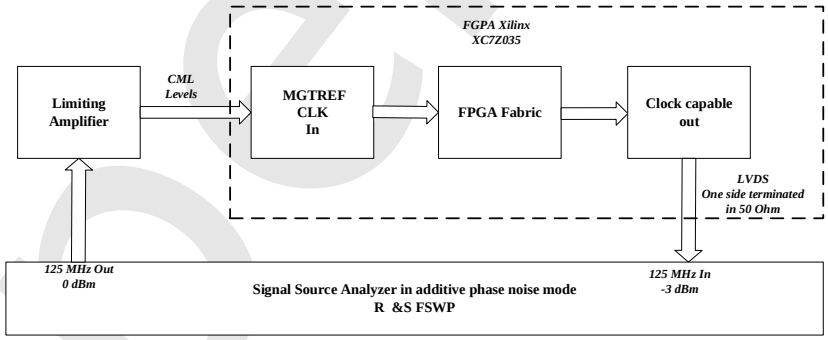


Figure 5: Test setup block schematic additive phase-noise.

in the following table 4 are the status shown of the fpga where the additive phase is on measured

| Trace number | FPGA configuration |
|---|---|
| 1 | MGT clock in routed to a clock capable output |
| 2 | FPGA loaded with CRC generator logic held in reset |
| 3 | FPGA loaded with CRC gererator logic working |

Table 4: FPGA configuration

In the following graph 6 is the result shown. It can been seen for the trace 1 & 2 and trace 3 that there is no increased of additive phase noise for offsets till 1/f corner frequency of $1e6Hz$ For trace 3 where the logic is full working there is after the corner frequeny a slight increase of the white noise floor. It seems that the jitter of the input ore output buffers dominating.this concclusion is based that there is not a lot of difference is between the state logic and only a clock pass-through.

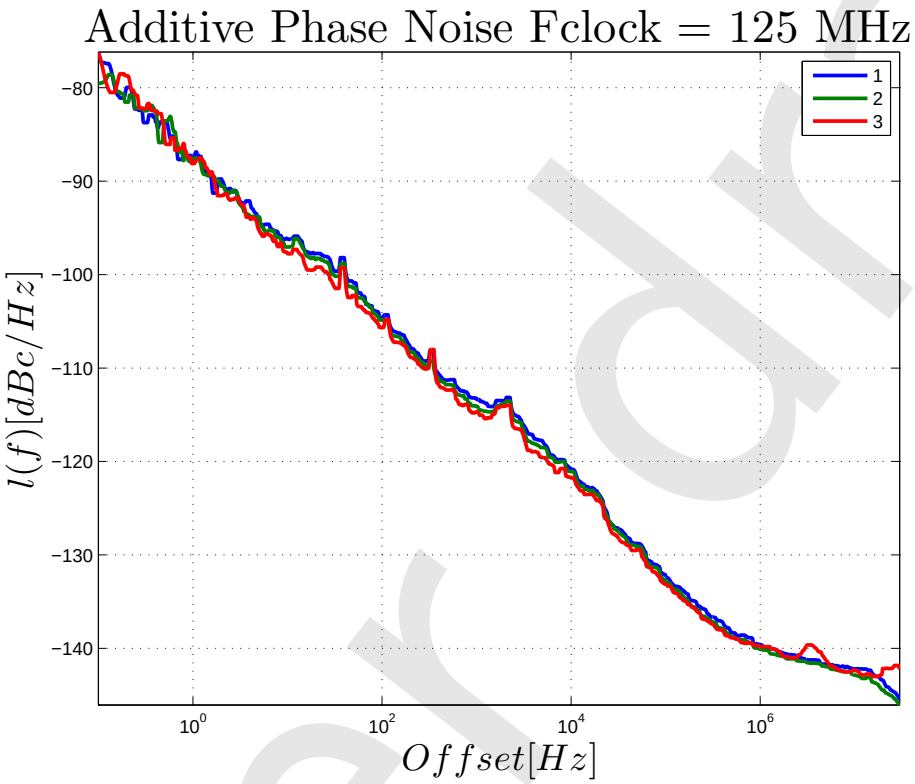


Figure 6: Result additive phase noise .

For reference the synthesized floor plan is shown in following figure 7 the highlighted (white) traces is the clock fabric Also the location where the clock is entering and leaving is shown in the figure see the red balloons.

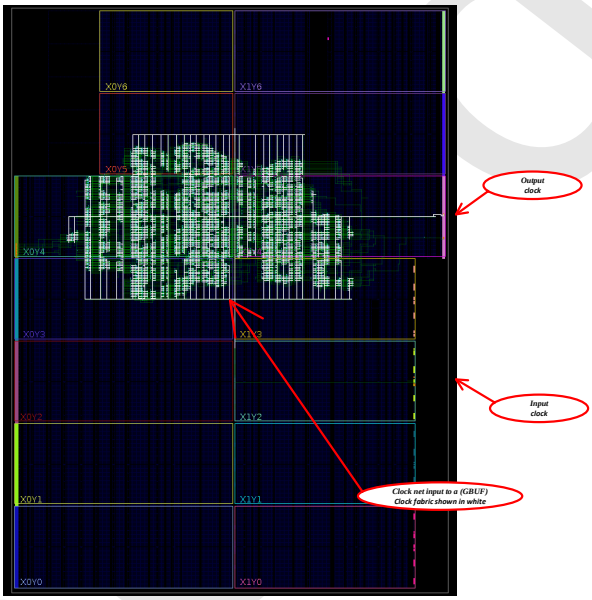


Figure 7: FPGA floor pan showing clock fabric.

# 3 Additive Phase noise limiting amplifiers

As a bonus the additive phase noise is has been determinate of the HMC914LP4E and LT6957-1 both from Analog Devices sine wave to square wave converter. This has been done with the FSWP additive phase noise option.both devices converting a sine wave to square wave.Both are limiting amplifiers (is is just a amplifier driving in compression).Where the HMC914 works up to 10GHz and the LT6957-1 to 500Mhz (at the input) the results are show in 8 and 9

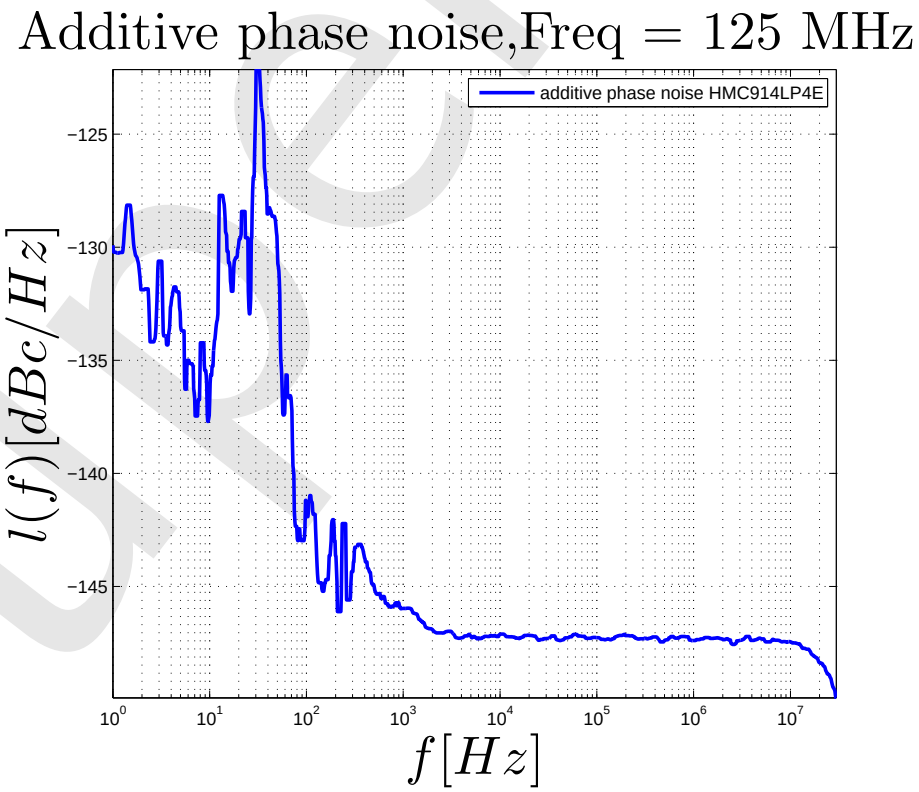


Figure 8: Additive phase noise HMC914LP4E.

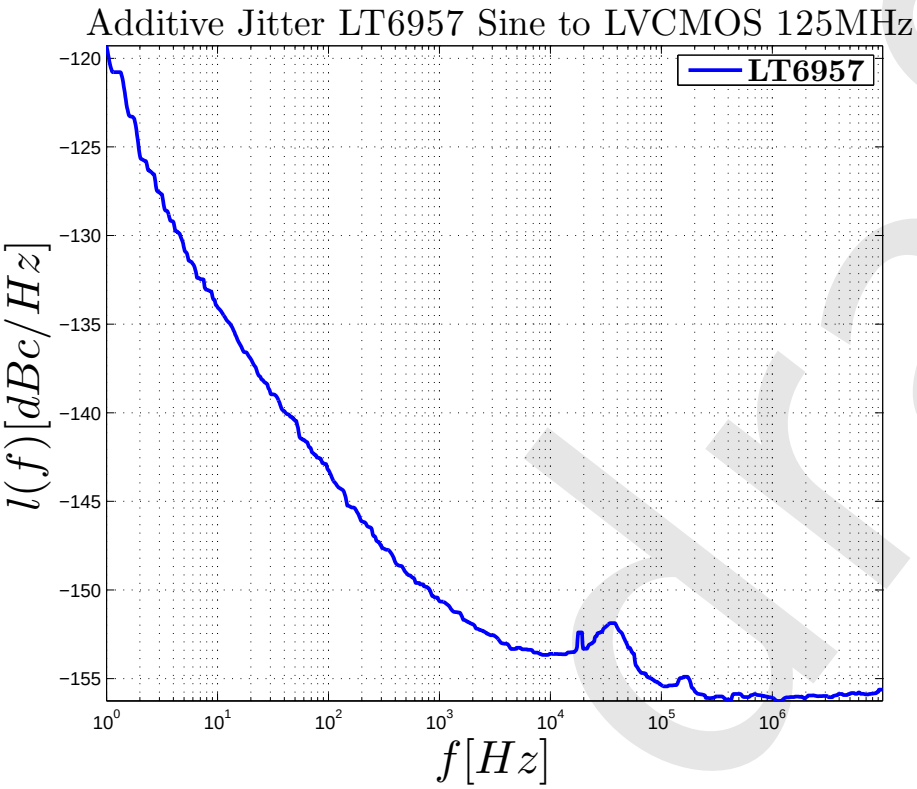


Figure 9: Additive phase noise LT6957-1.

| Item | Jitter $[fs]$ | Integration range |
|---|---|---|
| HMC914LP4E | 384,6244 | 1 to 30e6 $Hz$ |
| LT6957-1 | 91,842 | 1 to 10e6 $Hz$ |

Table 5: Additive Jitter 125 MHz

# List of Figures



# List of Tables