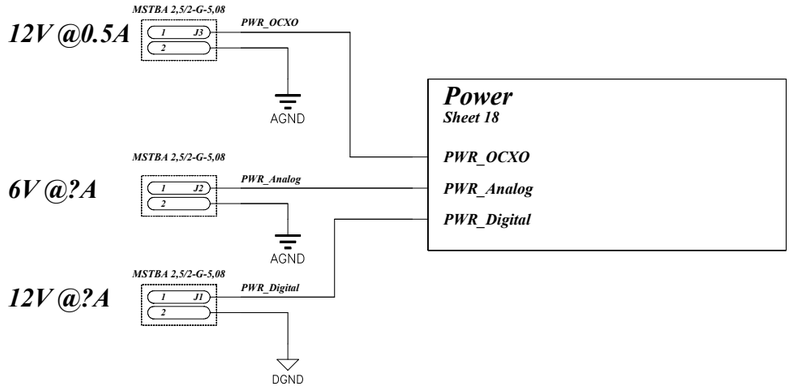

Power
Sheet 18
PWR_OCXO
PWR_Analog
PWR_Digital

FPGA_EEPROM_AND_JTAG
Sheet 8
JTAG
CONFIG
QSPI_BUS

WR_Clocks_IO And_Resample
Sheet 16
CLOCK_BUS

Clock_Out_Connectors
Sheet 15
CLOCK_BUS

CLOCK_BUS

External_SPI_test_Con
Sheet 2
SPI_EXT_TEST

SPI_EXT_TEST

FPGA_Spartan7
Sheet 4
SPI_EXT_TEST
LVDS_DAC
LVDS_SPI_PLL
JTAG
CONFIG
QSPI_BUS
DAC_LVCMOS
100MHZ_EXT_INT
PLL_SPI_LVCMOS
FPGA_CLK
SWITCH_LED

Digital_IO
Sheet 3
LVDS_DAC
LVDS_SPI_PLL

LVDS_DAC
LVDS_SPI_PLL
JTAG
CONFIG
QSPI_BUS
DAC_LVCMOS
100MHZ_EXT_INT
PLL_SPI_LVCMOS
FPGA_CLK
SWITCH_LED

ISO_SPI_DAC_PLL
Sheet 10
DAC_LVCMOS
100MHZ_EXT_INT
PLL_SPI_LVCMOS
FPGA_CLK
SPI_ISOLATED_DAC
ISO_100MHZ_EXT_INT
Coupled_CLK_IN
SPI_ISOLATED_PLL

SPI_ISOLATED_DAC
ISO_100MHZ_EXT_INT
Coupled_CLK
SPI_ISOLATED_PLL

OCXO_ASY
Sheet 12
SPI_ISOLATED_DAC
ISO_100MHZ_EXT_INT
Coupled_CLK
100MHz_Out

100MHz_Out

PLL_ASY
Sheet 14
100MHZ_Ref_IN_PLL
CLOCK_BUS
SPI_ISOLATED_PLL

Switch_and_led
Sheet 9
SWITCH_LED

MTG thru hole 3.2mm MH1 MH2 MH3 MH4 MH5 MH6 MH7 MH8 MH9 MH10 MH11 MH12 MH13 MH14 MH15 MH16 MH17 MH18

rev.	by	notes

100MHz in the loop

Project : ET Pathfinder demonstrator
Sheetname : Schematic1

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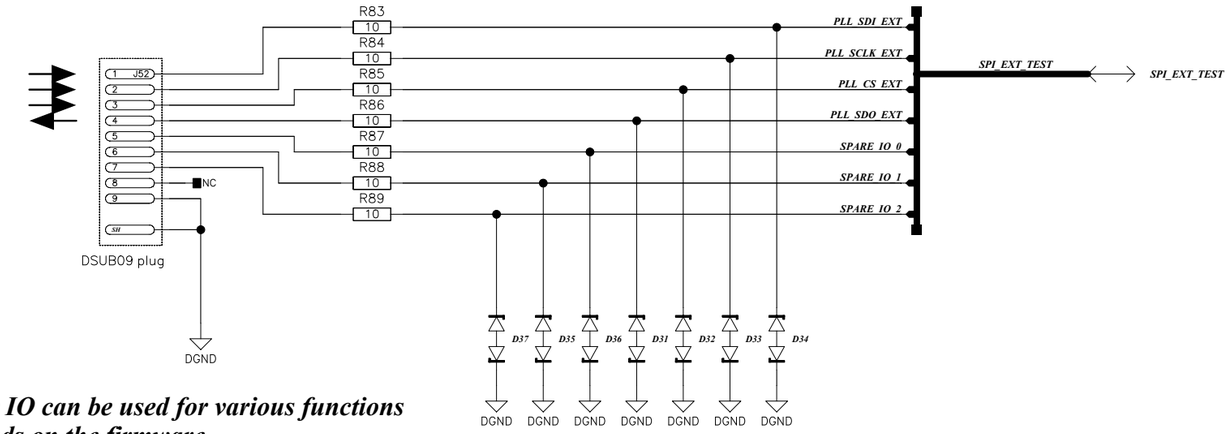
Sheet: 1 of 20 A3
Date: 2021-08-23

Test connector to hookup a microcrontroller.
LVCMOS 3V3! No buffers direct to the FPGA.



Spare IO can be used for various functions depends on the firmware.
Signal direction depends on firmware

rev.	by	notes

100MHz in the loop

Project : ***ET Pathfinder demonstrator***

Sheetname : ***External_SPI_test_Con***

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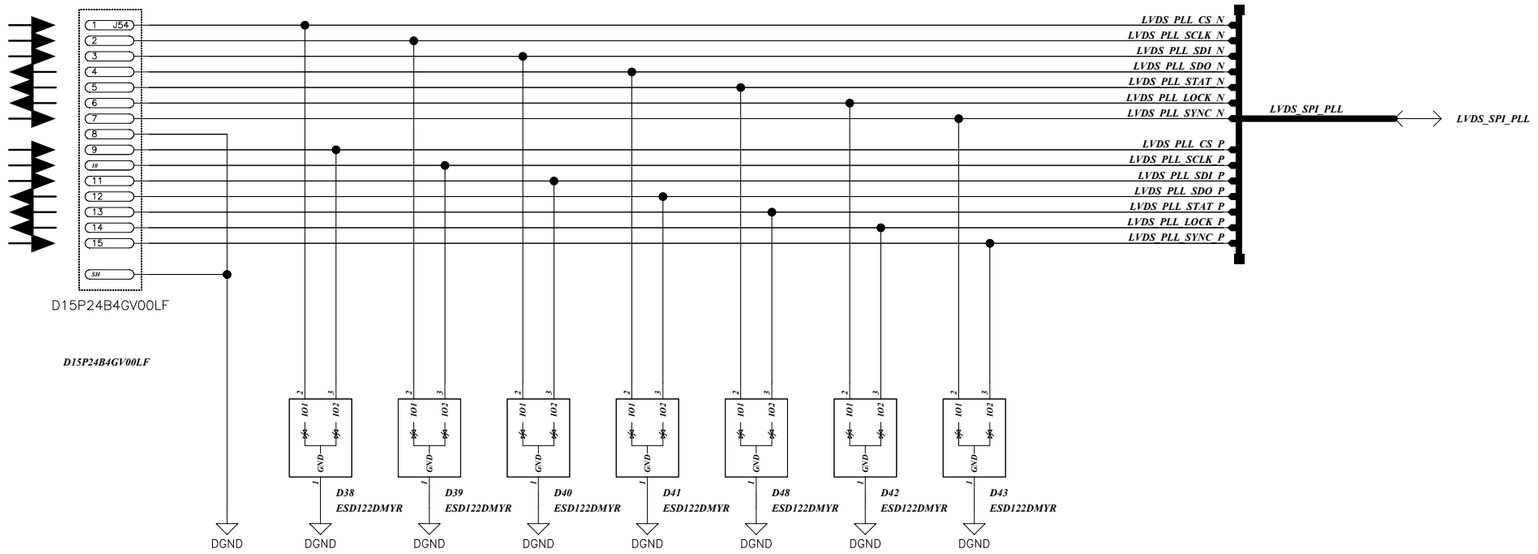
Sheet *2 of 20* *A3*

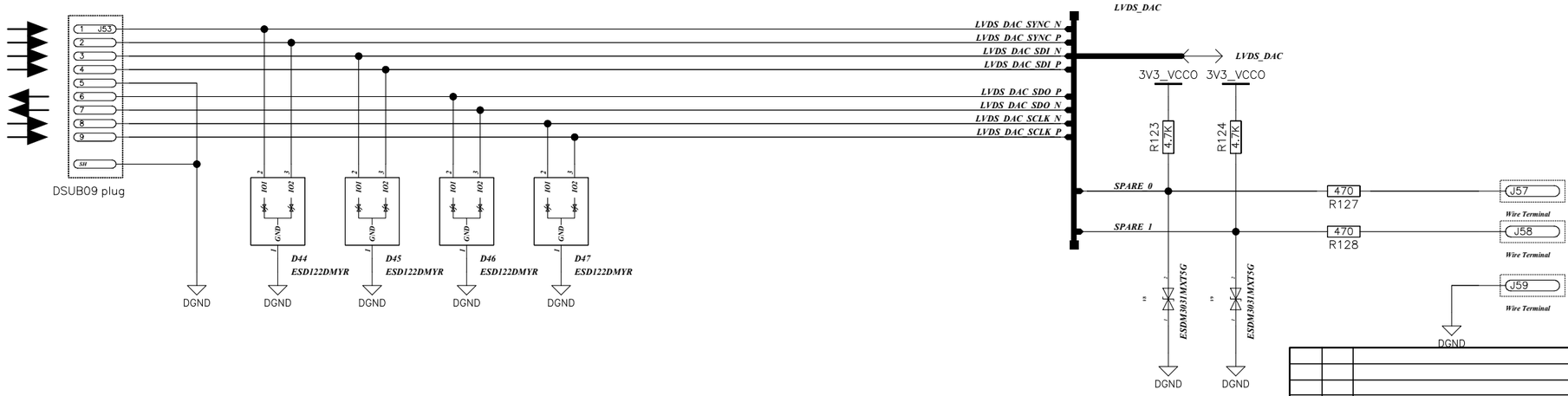
Date ***2021-08-23***

Connectors PLL Control & DAC



Text on Board => LVDS !

From WR. Tune Reference oscillator.



rev.	by	notes

100MHz in the loop

Project : ***ET Pathfinder demonstrator***

Sheetname : ***Digital_IO***

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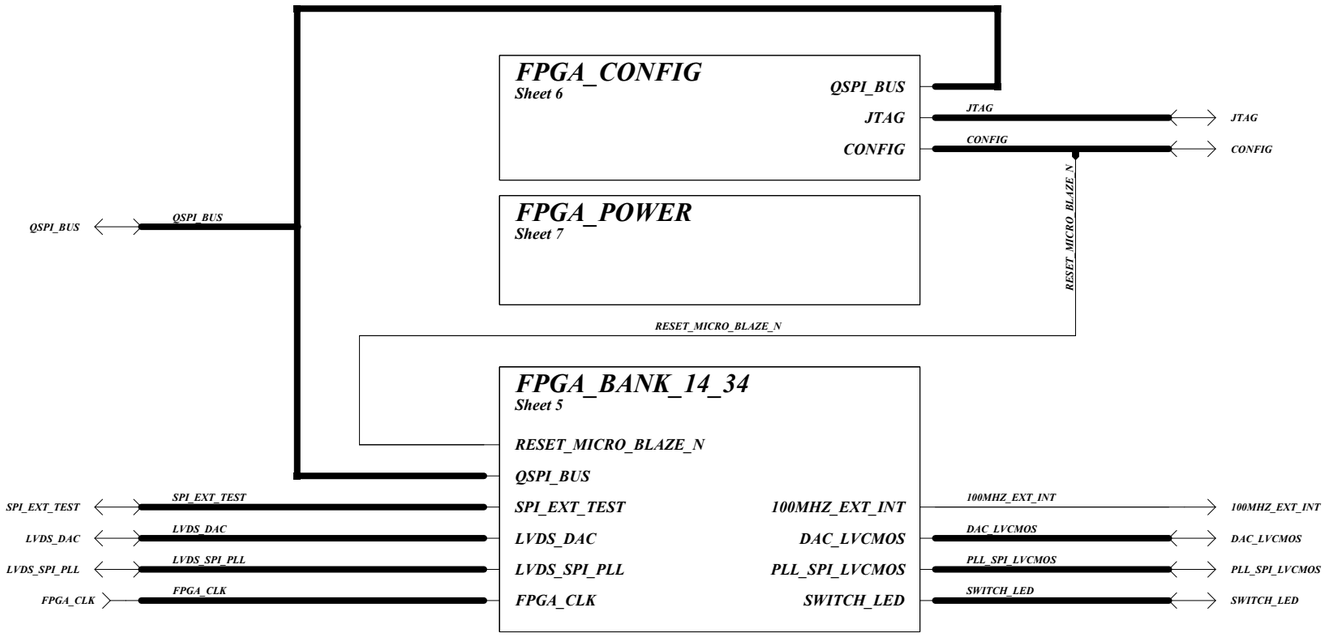
Size ***420 x 297mm*** ***A3***

Sheet ***3 of 20***

Date ***2021-08-23***



rev.	by	notes

100MHz in the loop

Project	: ET Pathfinder demonstrator
Sheetname	: FPGA_Spartan7

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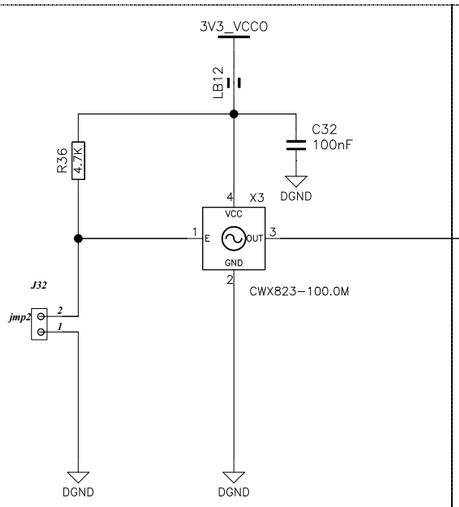
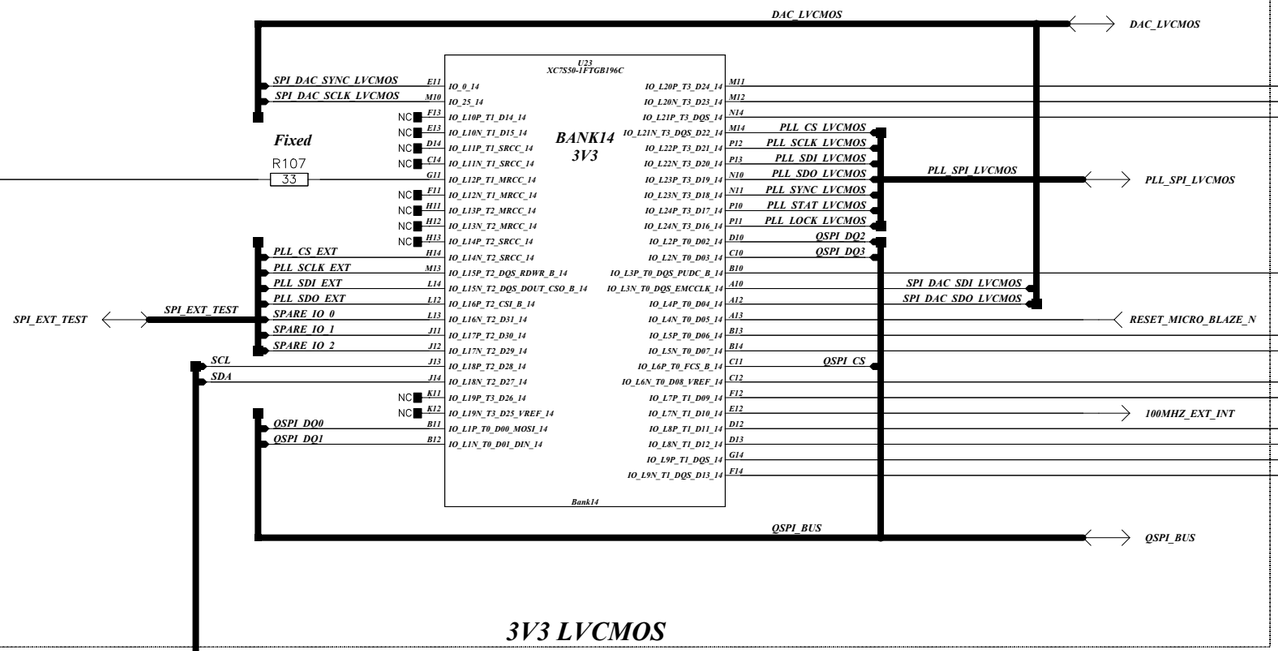
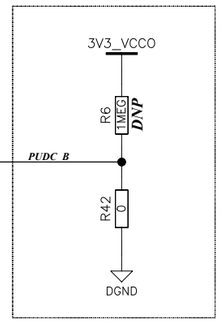
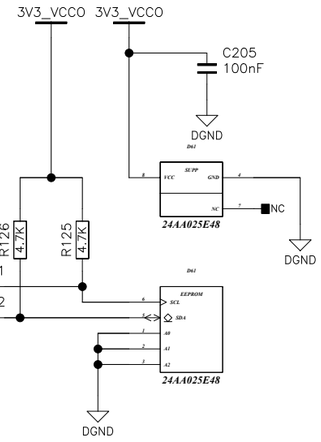


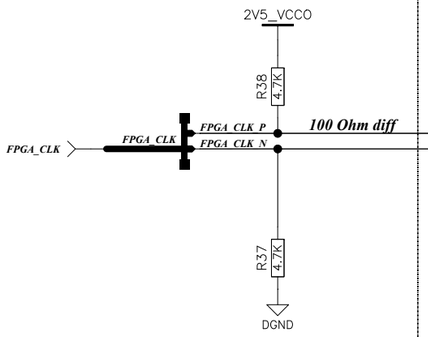
Backup 100MHz CLK
Place jumper to disable.



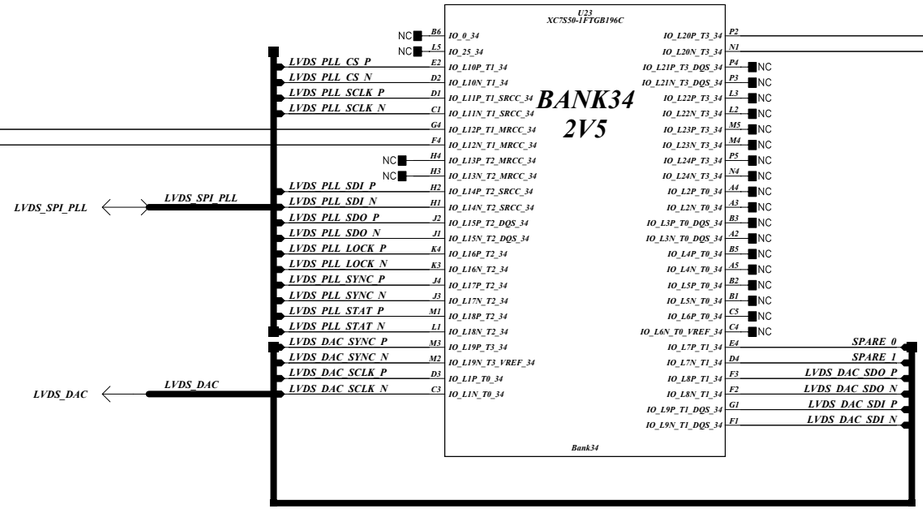


3V3 LVCMOS





FPGA_CLK is derived from the OCXO master,
so all internal clk are now phase related which
is benficial w.r.t. spurs and other unwanted "guests".
In normal use the "rescue" clk should be turn off.



2V5 LVDS

Note for Layout :
Nets can be swapped (respect bank volatge).
However, there are some exceptions:
mrcc, srcc type pind and pins for the eeprom.

rev.	by	notes

100MHz in the loop

Project	: ET Pathfinder demonstrator
Sheetname	: FPGA_BANK_14_34

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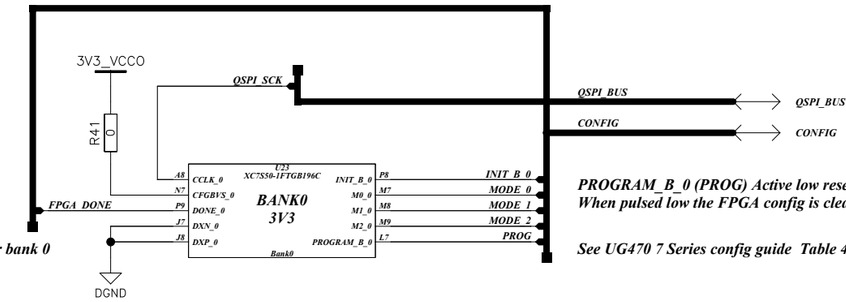
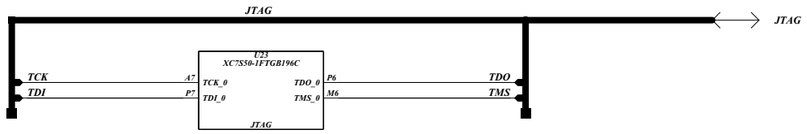


CFGBVS Pulled to 3V3 this pin selects the voltage IO for bank 0
See UG470 7 Series config guide Table 2-4

PROGRAM_B_0 (PROG) Active low reset.
When pulsed low the FPGA config is cleared and reloaded from FLASH.

See UG470 7 Series config guide Table 4-2



rev.	by	notes

100MHz in the loop

Project : ***ET Pathfinder demonstrator***

Sheetname : ***FPGA_CONFIG***

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Sheet ***6 of 20*** ***A3***

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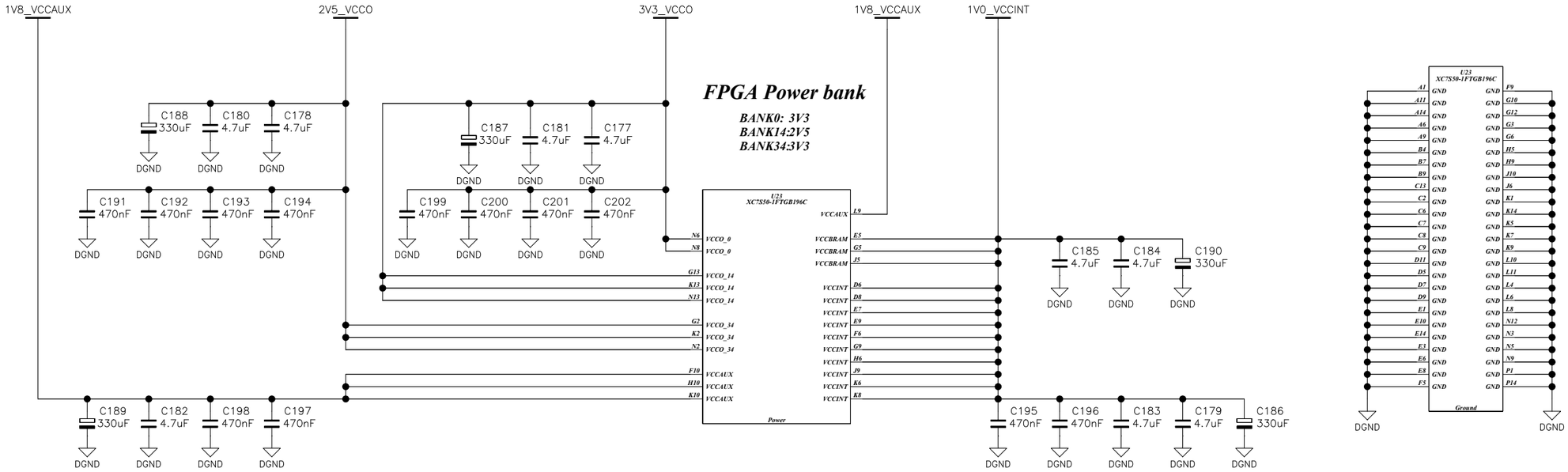
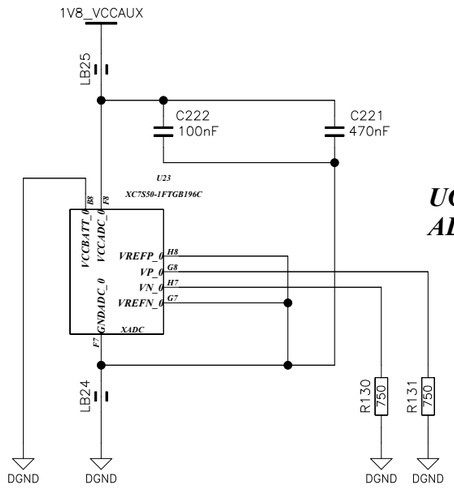


UG483 Table 2-1 (XC7S15 FTGB196):
VCCINT: 1x 100uF, 2x 4.7uF, 2x 0.47uF
VCCBRAM: 1x 47uF, 1x 4.7uF, 1x 0.47uF
VCCAUX: 1x 47uF, 1x 4.7uF, 2x 0.47uF
VCCO: 1x 47uF, 2x 4.7uF, 4x 0.47uF



DS189 Table 2 note 9
If battery is not used, connect VCCBATT to either ground or VCCAUX

UG480 Figure 1-2
ADC is not used in this desgin

rev.	by	notes

100MHz in the loop

Project : ***ET Pathfinder demonstrator***
Sheetname : ***FPGA_POWER***

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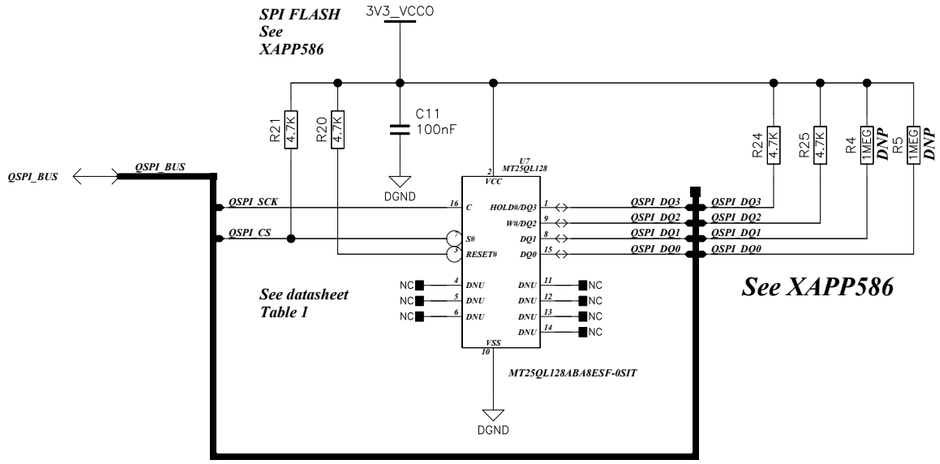
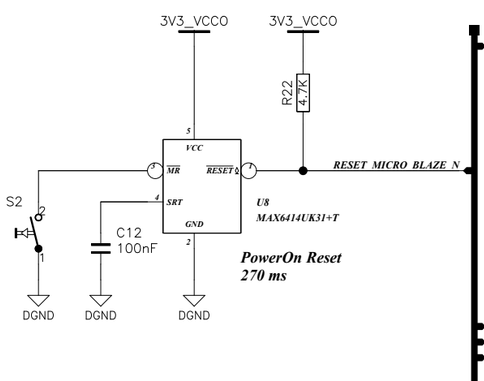
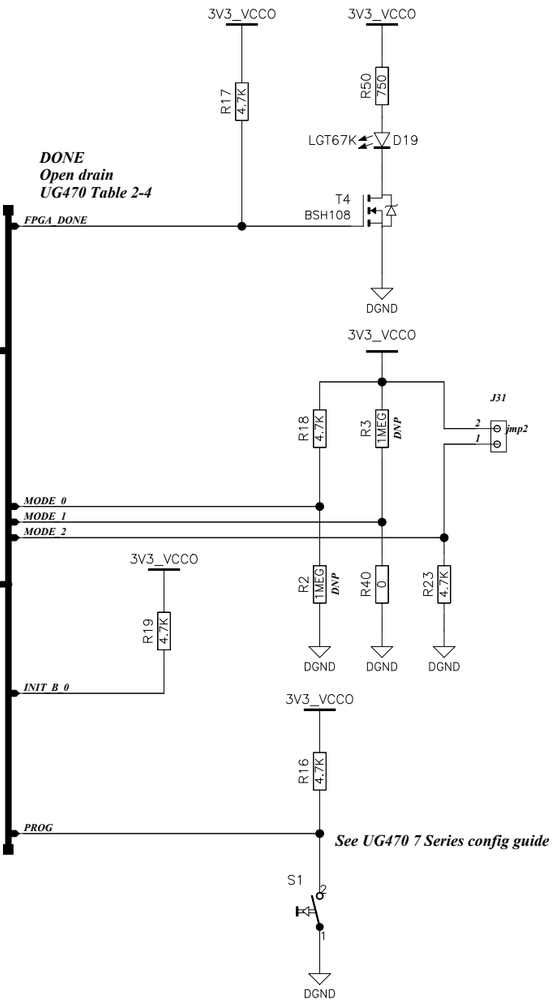
Date ***2021-08-23***



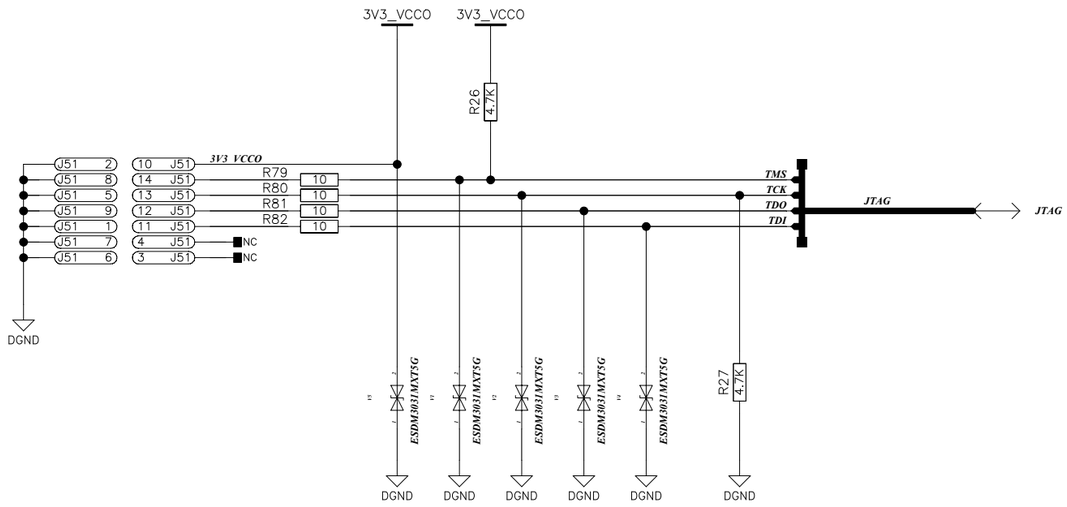




UG470 Table 2-1

Configuration mode	M2	M1	M0	Bush With
Master Serial	0	0	0	x1
Master SPI	0	0	1	x1,x2,x4
Master BPI	0	1	0	x8,x16
	0	1	1	
Master SelectMap	1	0	0	x8,x16
JTAG	1	0	1	x1
Slave SelectMap	1	1	0	x8,x16,x32
Slave Serial	1	1	1	x1

UG470 Table 2-1



ESD protection

rev.	by	notes

100MHz in the loop

Project	: ET Pathfinder demonstrator
Sheetname	: FPGA_EEPROM_AND_JTAG

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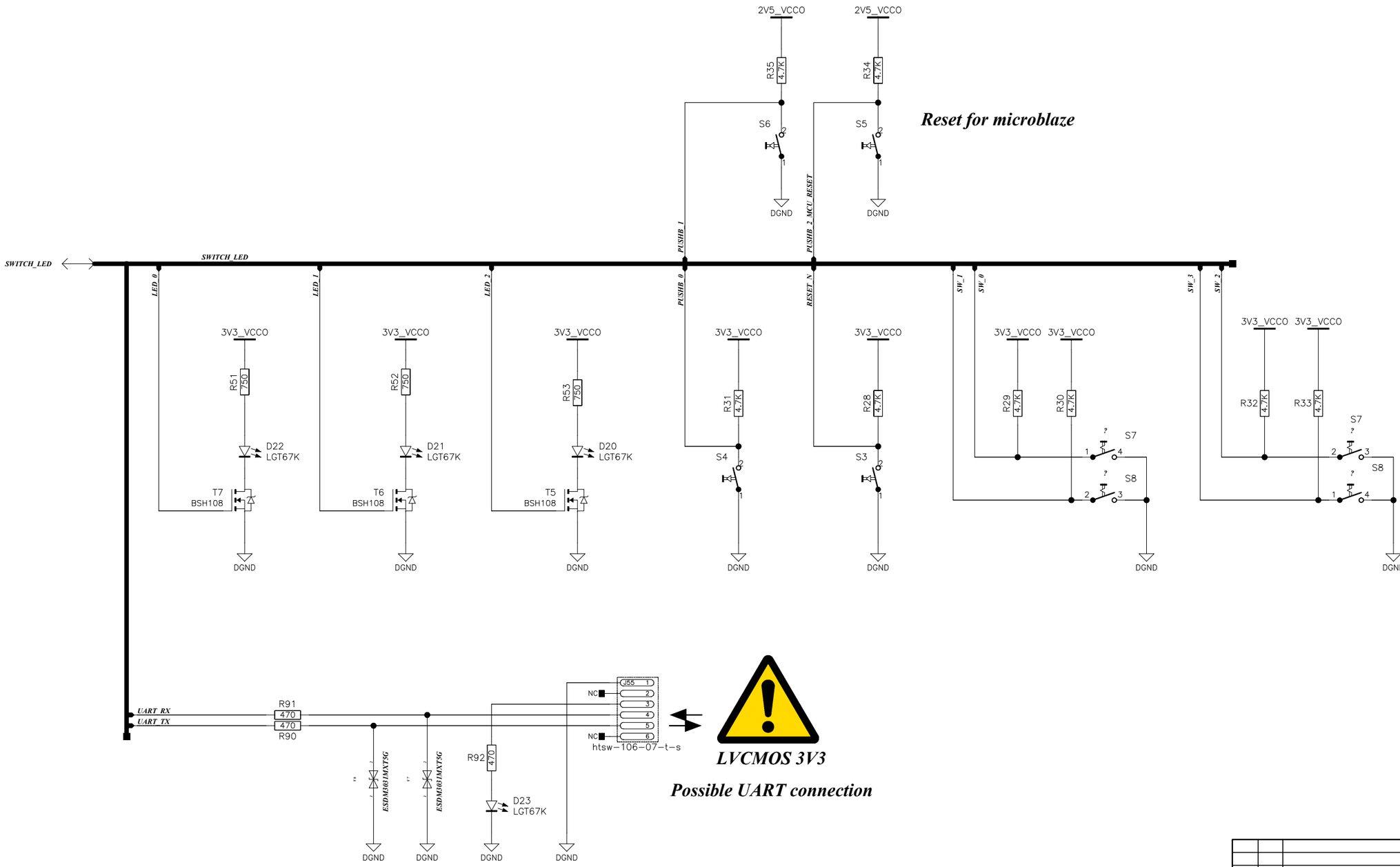
Date	2021-08-23



rev.	by	notes

100MHz in the loop

Project	: ET Pathfinder demonstrator
Sheetname	: Switch_and_led

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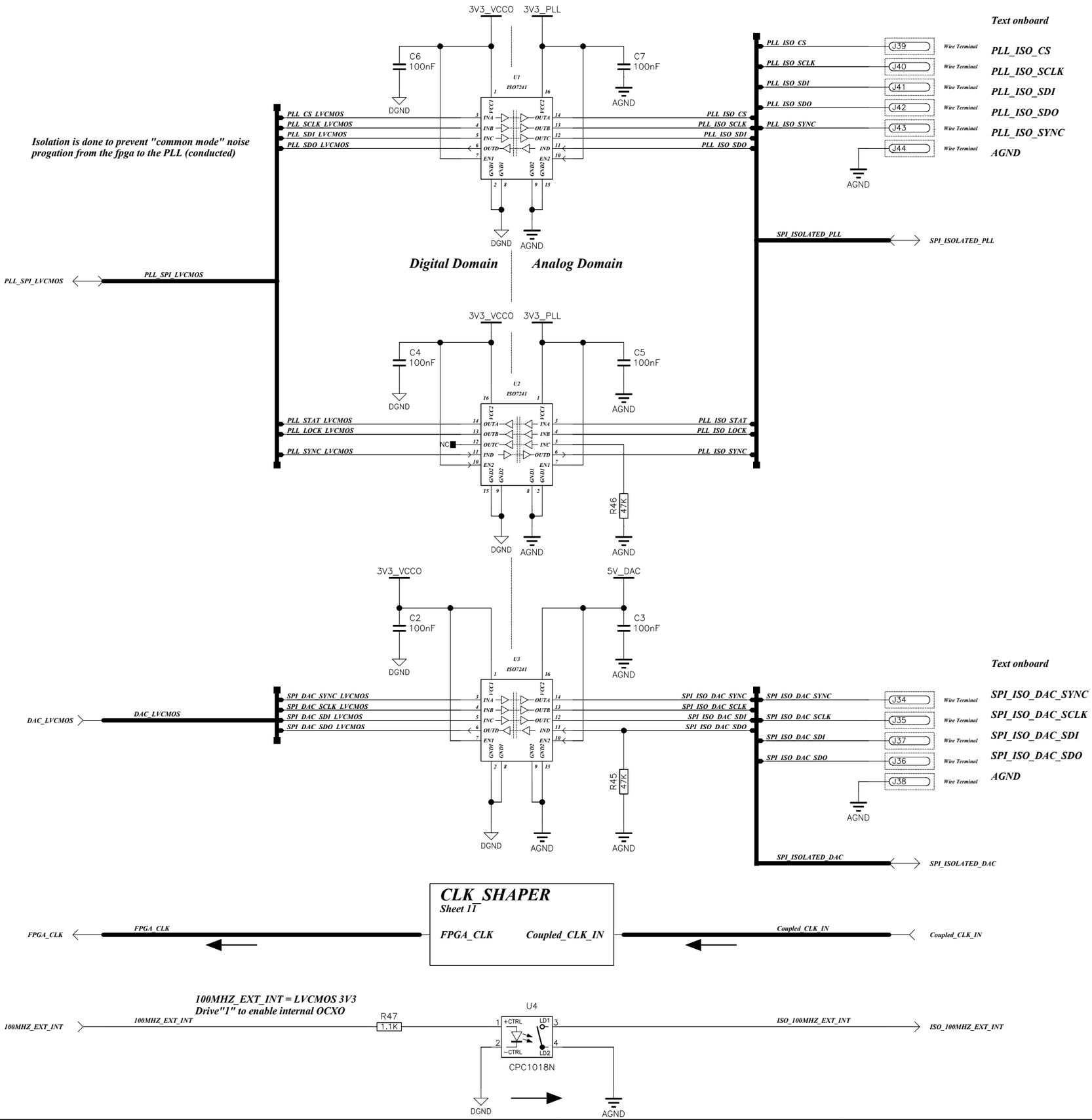
Sheet	9 of 20 A3
Date	2021-08-23



rev.	by	notes

100MHz in the loop

Project	: ET Pathfinder demonstrator
Sheetname	: ISO_SPI_DAC_PLL

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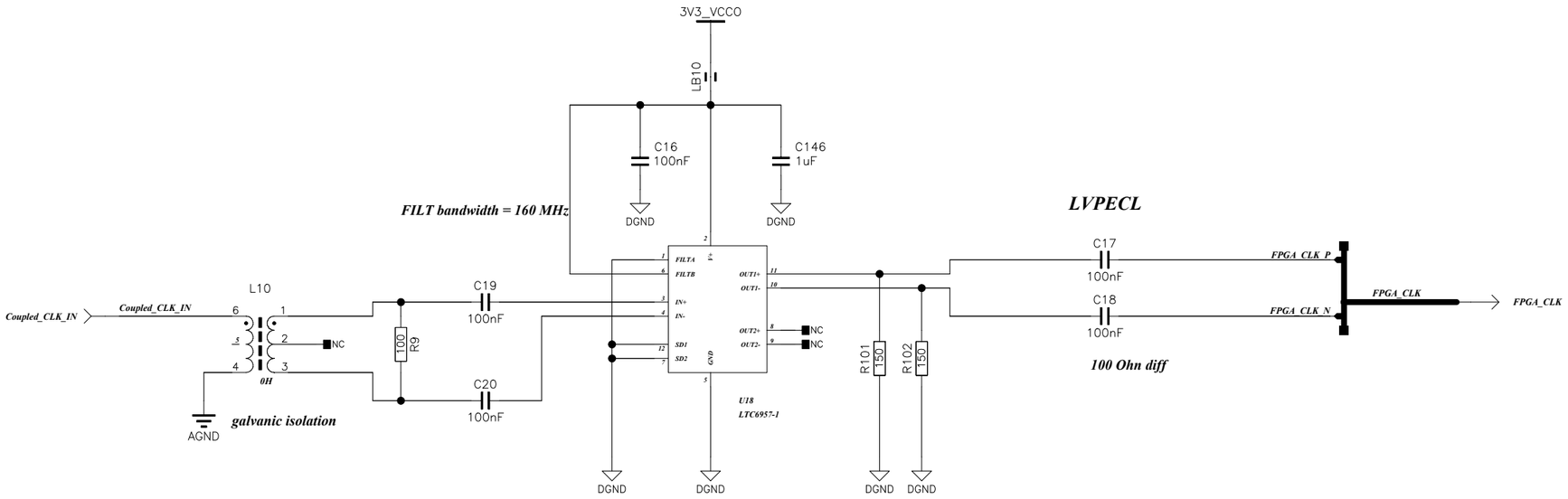
Size	420 x 297mm
Sheet	10 of 20 A3
Date	2021-08-23



FPGA clk Shaphing and isolating

rev.	by	notes

100MHz in the loop

Project	: ET Pathfinder demonstrator
Sheetname	: CLK_SHAPER

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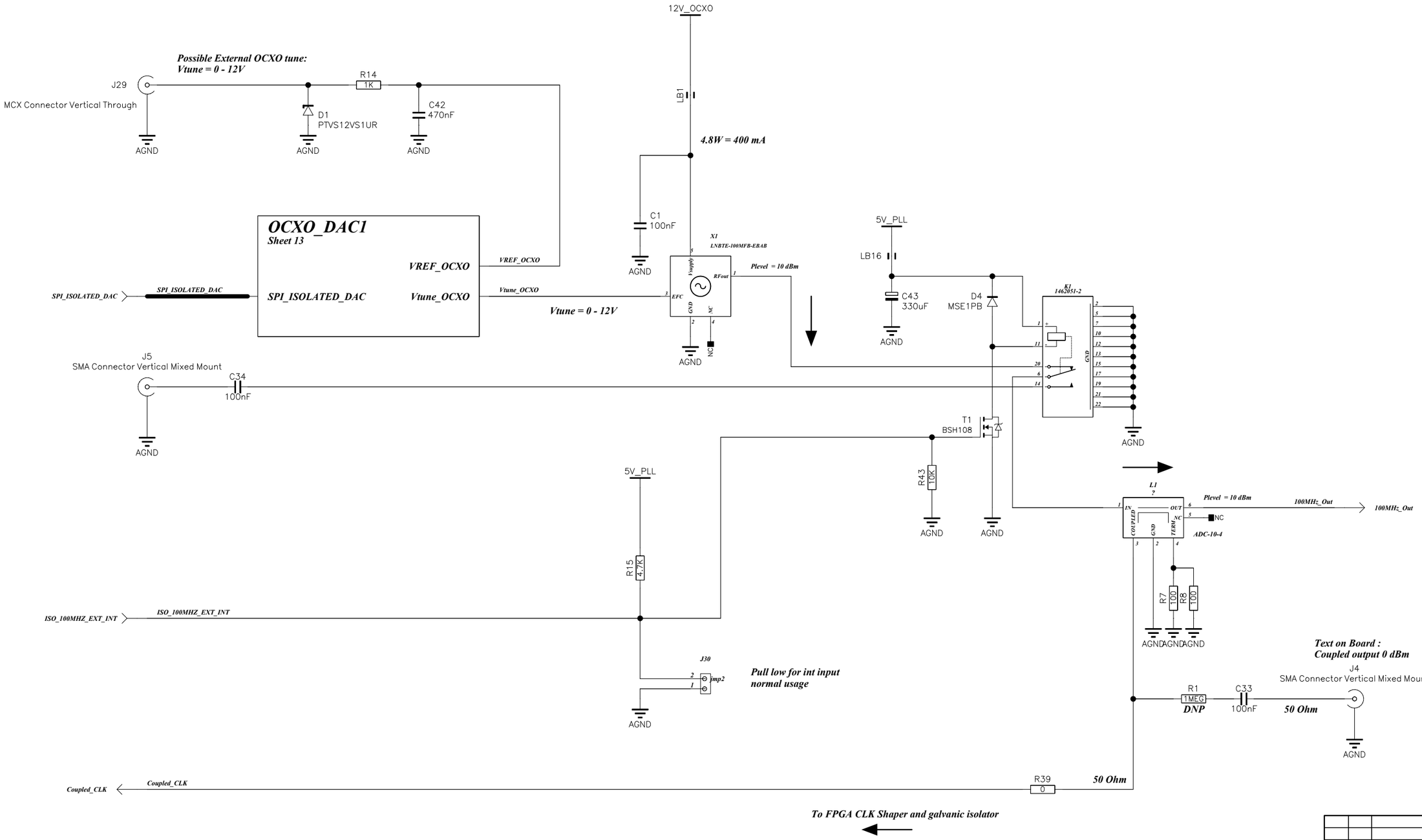
Sheet	11 of 20 A3
Date	2021-08-23



rev.	by	notes

100MHz in the loop

Project	: ET Pathfinder demonstrator
Sheetname	: OCXO_ASY

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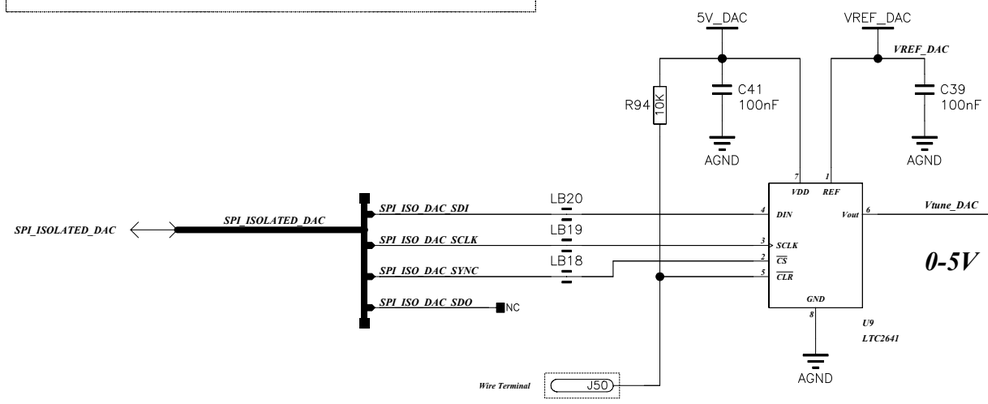
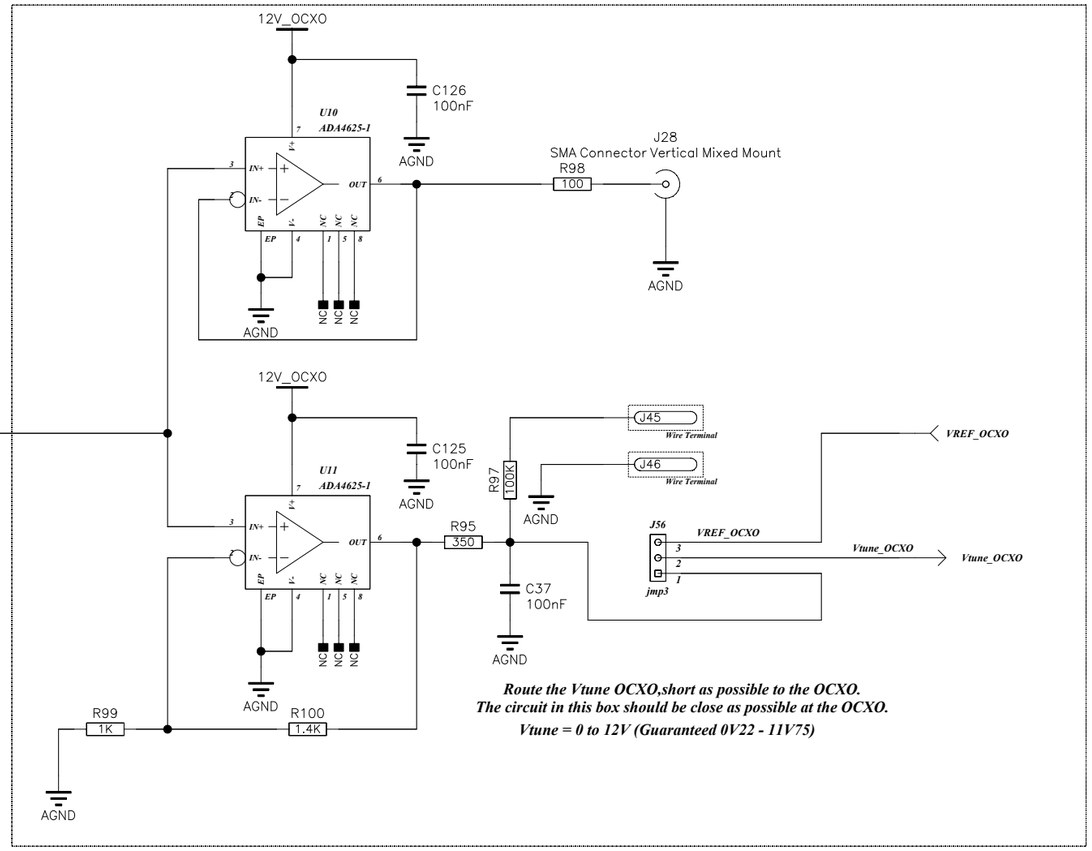
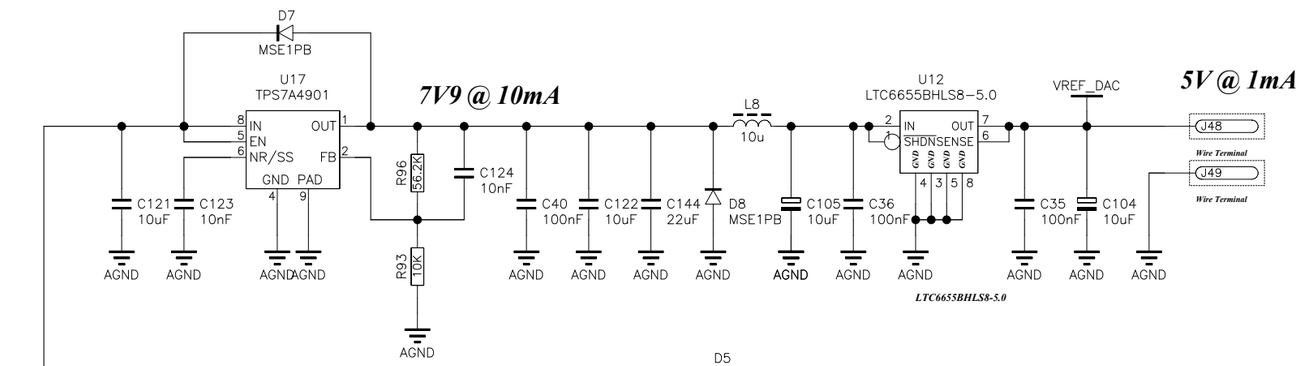
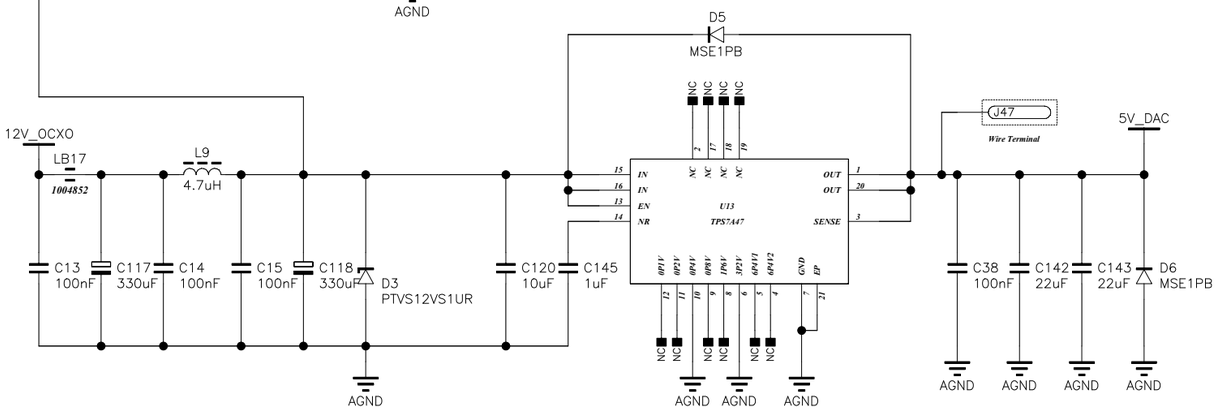
Date	2021-08-23

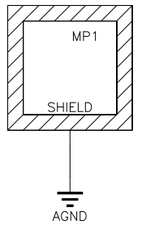
Place all componest under the shielded can, to shield it from EMI, and reduce the airflow around this circuit

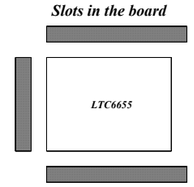












rev.	by	notes

100MHz in the loop

Project	***: ET Pathfinder demonstrator***
Sheetname	***: OCXO_DAC***

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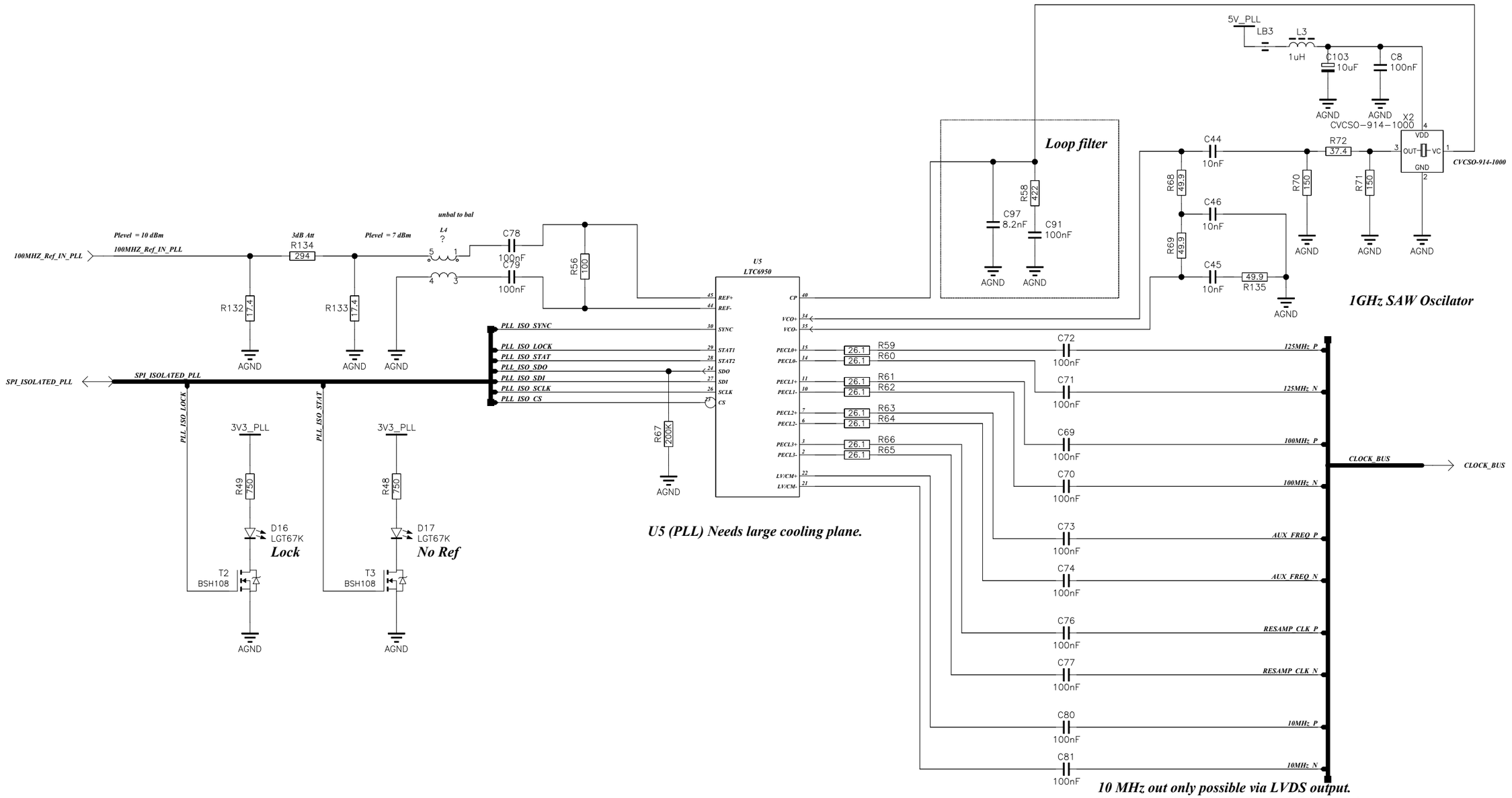
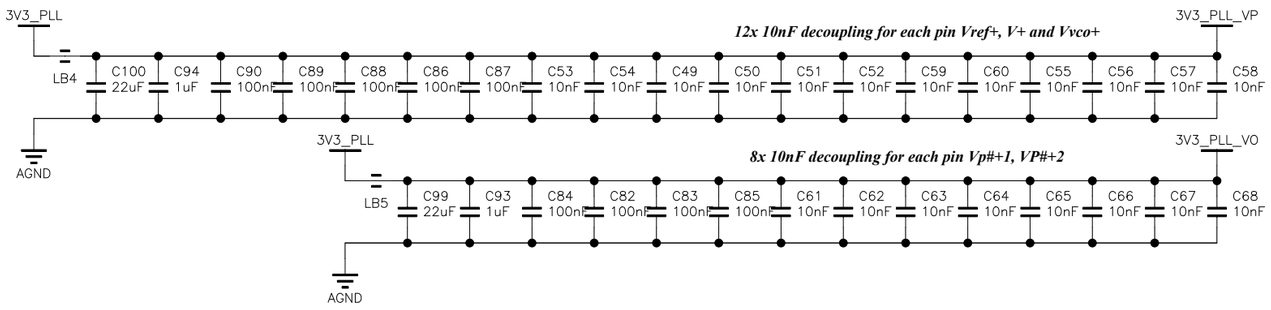
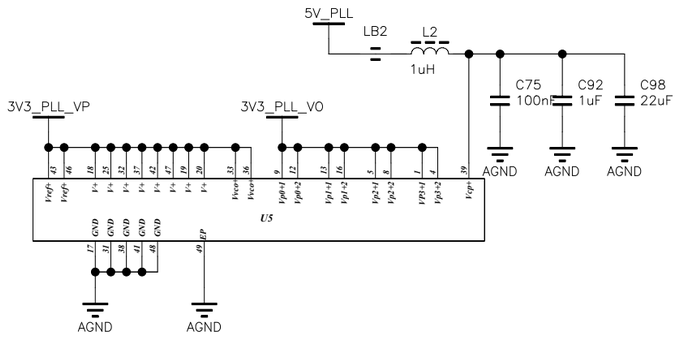
Date	***2021-08-23***







rev.	by	notes
		100MHz in the loop

Project	: ET Pathfinder demonstrator
Sheetname	: PLL_ASY

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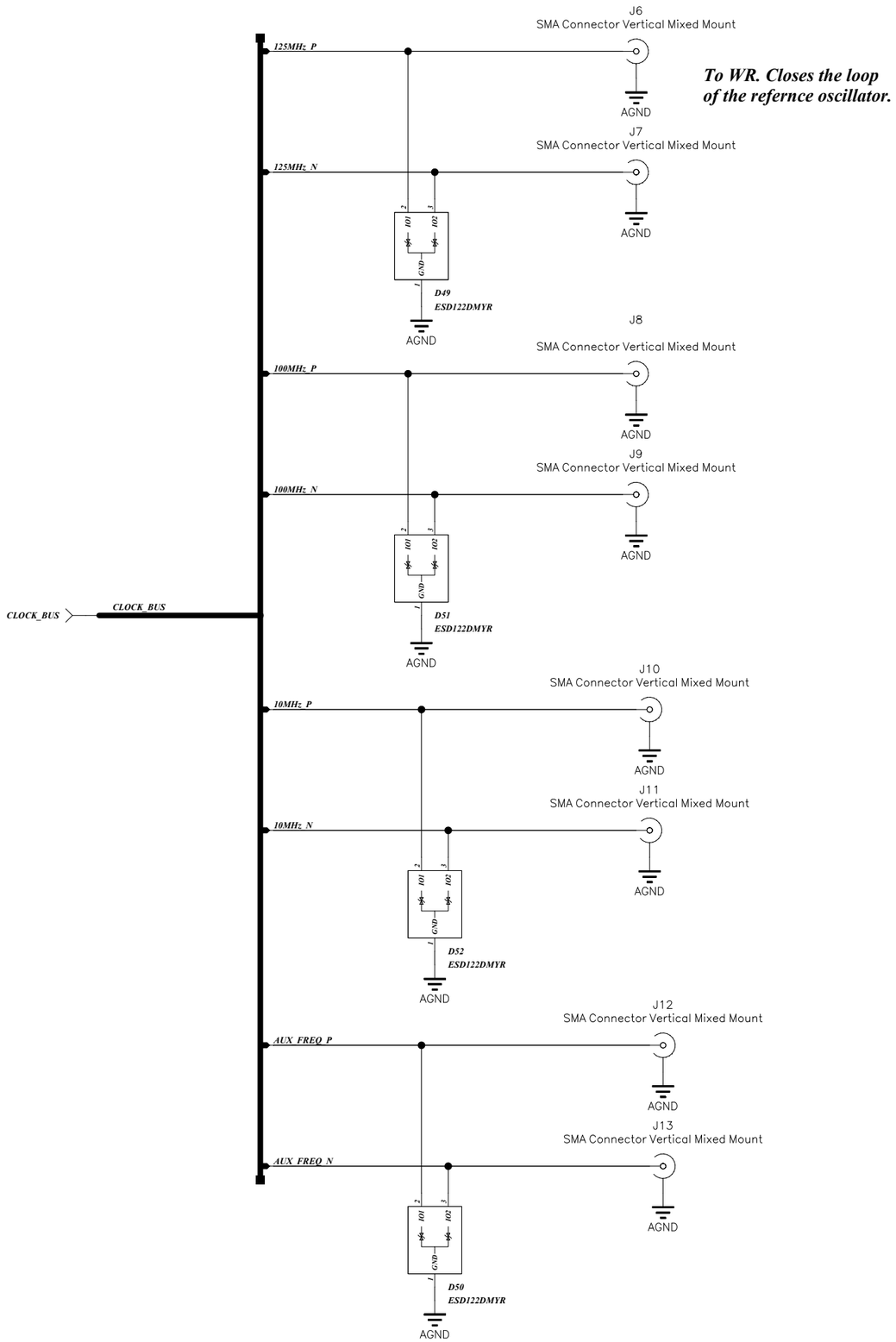

rev.	by	notes

100MHz in the loop

Project	: ET Pathfinder demonstrator
Sheetname	: Clock_Out_Connectors

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Sheet	15 of 20 A3
Date	2021-08-23

CLOCKS From WR
Phase aligned with WR
125 MHz reference clock.

J14
SMA Connector Vertical Mixed Mount
AGND
CLK_FROM_WR_P

J15
SMA Connector Vertical Mixed Mount
AGND
CLK_FROM_WR_N

D53
ESD122DMYR
AGND

1 PPS DC coupled!

J16
SMA Connector Vertical Mixed Mount
AGND
1PPS_FROM_WR_P

J17
SMA Connector Vertical Mixed Mount
AGND
1PPS_FROM_WR_N

D54
ESD122DMYR
AGND

J60
SMA Connector Vertical Mixed Mount
AGND
CLK_FROM_WR_2_P

J61
SMA Connector Vertical Mixed Mount
AGND
CLK_FROM_WR_2_N

D62
ESD122DMYR
AGND

J18
SMA Connector Vertical Mixed Mount
AGND
TEST_INPUT_P

J19
SMA Connector Vertical Mixed Mount
AGND
TEST_INPUT_N

D55
ESD122DMYR
AGND

CLOCK_BUS

CLOCKS_WR
CLOCK_BUS

Resampler
Sheet 17
CLOCKS_WR CLOCKS_WR_RESAMPLED
CLOCK_BUS
CLOCKS_WR_RESAMPLED_SPARE

CLOCKS_WR_RESAMPLED
CLOCKS_WR_RESAMPLED_SPARE

Resampled Clk and
1 PPS from WR

J20
SMA Connector Vertical Mixed Mount
AGND
CLK_FROM_WR_RESAMPLED_P

Clk is AC
coupled CML!

J21
SMA Connector Vertical Mixed Mount
AGND
CLK_FROM_WR_RESAMPLED_N

D56
ESD122DMYR
AGND

J22
SMA Connector Vertical Mixed Mount
AGND
1PPS_FROM_RESAMPLED_WR_P

1 PPS is LVPECL
DC Coupled!

J23
SMA Connector Vertical Mixed Mount
AGND
1PPS_FROM_RESAMPLED_WR_N

D57
ESD122DMYR
AGND

J26
SMA Connector Vertical Mixed Mount
AGND
CLK_FROM_WR_RESAMPLED_2_P

J27
SMA Connector Vertical Mixed Mount
AGND
CLK_FROM_WR_RESAMPLED_2_N

D59
ESD122DMYR
AGND

J24
SMA Connector Vertical Mixed Mount
AGND
RESAMPLER_CLK_SPARE0_P
C209
100nF

J25
SMA Connector Vertical Mixed Mount
AGND
RESAMPLER_CLK_SPARE0_N
C210
100nF

D58
ESD122DMYR
AGND

rev.	by	notes

100MHz in the loop

Project : ET Pathfinder demonstrator
Sheetname : WR_CLOCKS_IO

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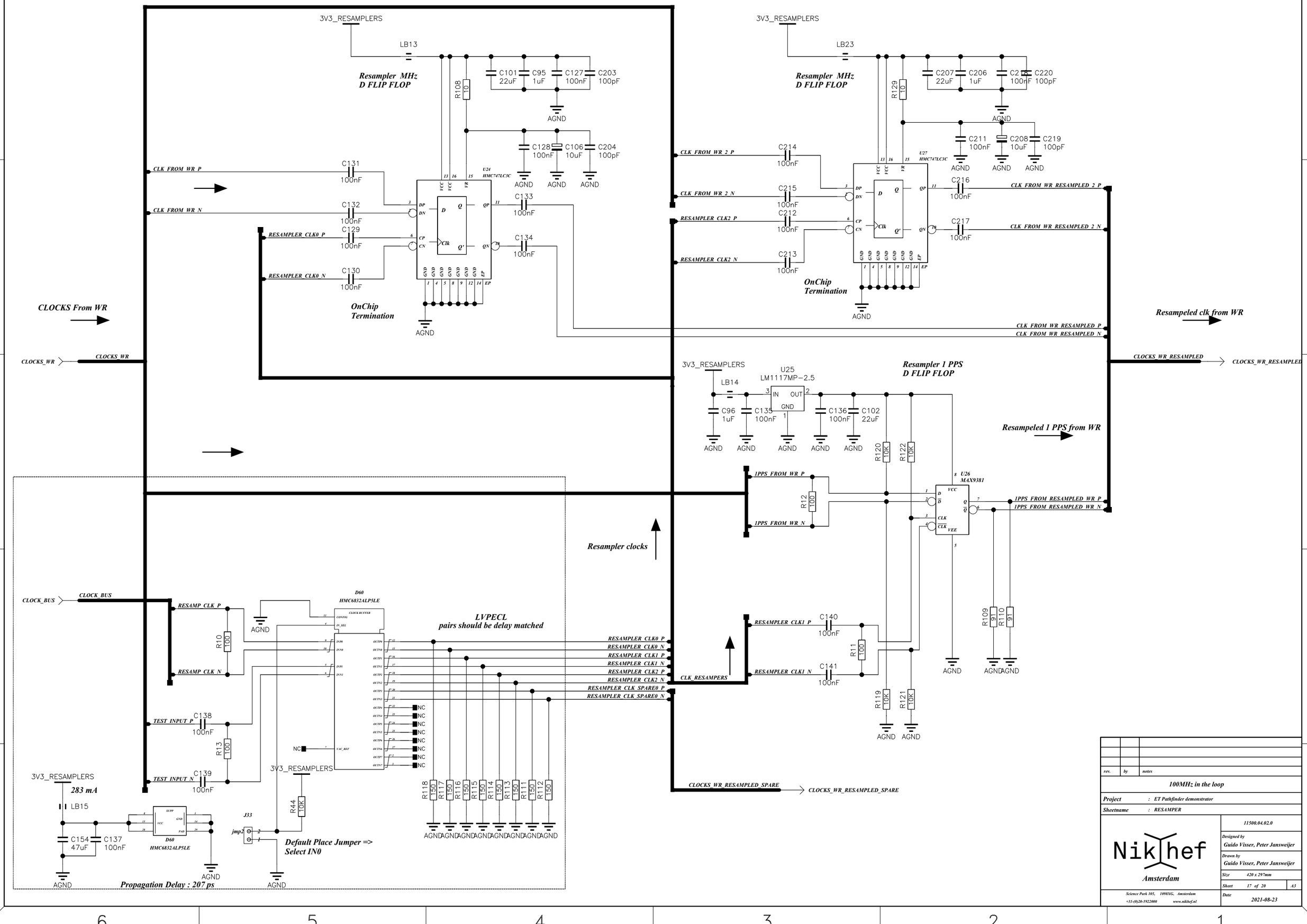
11500.04.02.0
Designed by: Guido Visser, Peter Jansweijer
Drawn by: Guido Visser, Peter Jansweijer
Size: 420 x 297mm
Sheet: 16 of 20 A3
Date: 2021-08-23


3V3_RESAMPLERS
LB13
Resampler MHz
D FLIP FLOP
R108
10
C101 22uF
C95 1uF
C127 100nF
C203 100pF
AGND
C128 100nF
C106 10uF
C204 100pF
CLK_FROM_WR_P
CLK_FROM_WR_N
RESAMPLER_CLK0_P
RESAMPLER_CLK0_N
C131 100nF
C132 100nF
C129 100nF
C130 100nF
U24
HMC747LC3C
C133 100nF
C134 100nF
OnChip
Termination
CLOCKS From WR
CLOCKS_WR
3V3_RESAMPLERS
LB23
Resampler MHz
D FLIP FLOP
R129
10
C207 22uF
C206 1uF
C205 100nF
C220 100pF
C211 100nF
C208 10uF
C219 100pF
CLK_FROM_WR_2_P
CLK_FROM_WR_2_N
RESAMPLER_CLK2_P
RESAMPLER_CLK2_N
C214 100nF
C215 100nF
C212 100nF
C213 100nF
U27
HMC747LC3C
C216 100nF
C217 100nF
CLK_FROM_WR_RESAMPLED_2_P
CLK_FROM_WR_RESAMPLED_2_N
OnChip
Termination
CLK_FROM_WR_RESAMPLED_P
CLK_FROM_WR_RESAMPLED_N
Resampeled clk from WR
CLOCKS_WR_RESAMPLED
CLOCKS_WR_RESAMPLED
3V3_RESAMPLERS
LB14
U25
LM1117MP-2.5
C96 1uF
C135 100nF
C136 100nF
C102 22uF
Resampler 1 PPS
D FLIP FLOP
Resampeled 1 PPS from WR
R120 10K
R122 10K
1PPS_FROM_WR_P
1PPS_FROM_WR_N
R12 100
U26
MAX9381
1PPS_FROM_RESAMPLED_WR_P
1PPS_FROM_RESAMPLED_WR_N
Resampler clocks
CLOCK_BUS
CLOCK_BUS
RESAMP_CLK_P
RESAMP_CLK_N
R10 100
D60
HMC6832ALP5LE
LVPECL
pairs should be delay matched
RESAMPLER_CLK0_P
RESAMPLER_CLK0_N
RESAMPLER_CLK1_P
RESAMPLER_CLK1_N
RESAMPLER_CLK2_P
RESAMPLER_CLK2_N
RESAMPLER_CLK_SPARE0_P
RESAMPLER_CLK_SPARE0_N
CLK_RESAMPERS
RESAMPLER_CLK1_P
RESAMPLER_CLK1_N
C140 100nF
C141 100nF
R11 100
R109 91
R110 91
R119 10K
R121 10K
TEST_INPUT_P
TEST_INPUT_N
C138 100nF
C139 100nF
R13 100
3V3_RESAMPLERS
283 mA
LB15
C154 47uF
C137 100nF
D60
HMC6832ALP5LE
J33
jmp2
R44 10K
Default Place Jumper =>
Select IN0
Propagation Delay : 207 ps
R118 150
R117 150
R116 150
R115 150
R114 150
R113 150
R111 150
R112 150
CLOCKS_WR_RESAMPLED_SPARE
CLOCKS_WR_RESAMPLED_SPARE
rev. by notes
100MHz in the loop
Project : ET Pathfinder demonstrator
Sheetname : RESAMPER
11500.04.02.0
Designed by
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Drawn by
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Size 420 x 297mm
Sheet 17 of 20
A3
Date
2021-08-23
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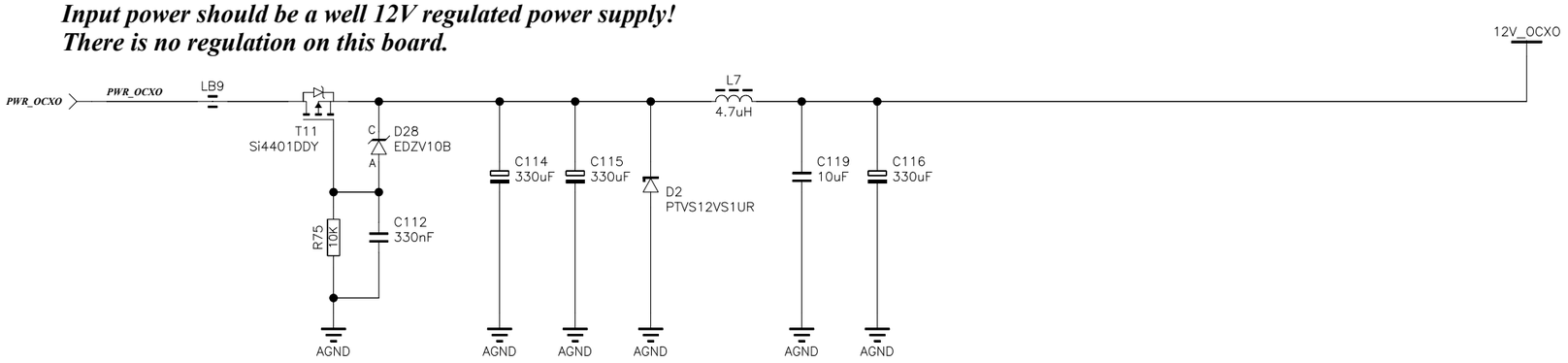
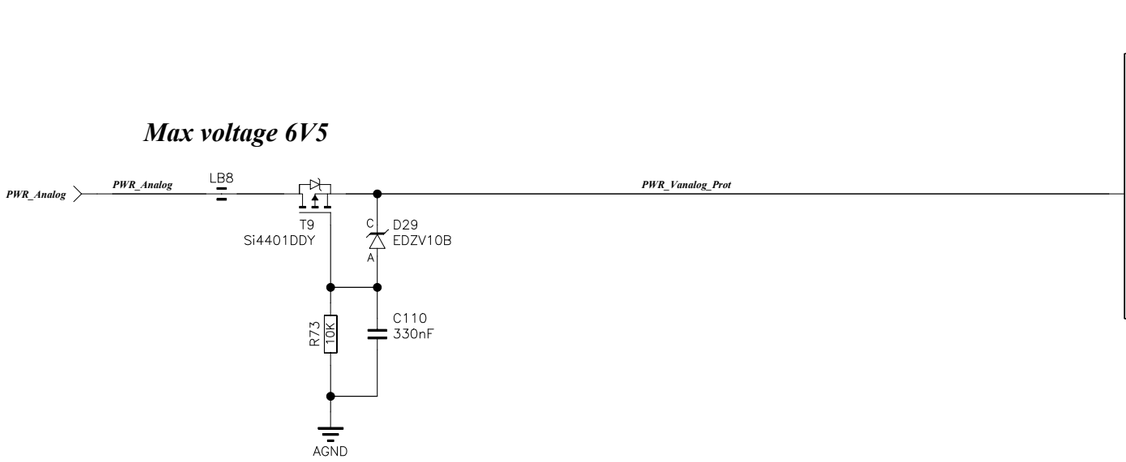
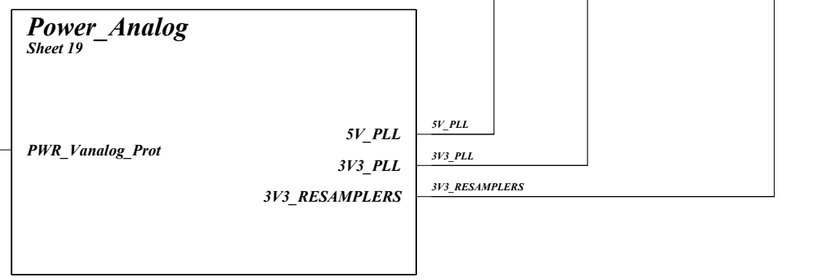
Input power should be a well 12V regulated power supply!
There is no regulation on this board.



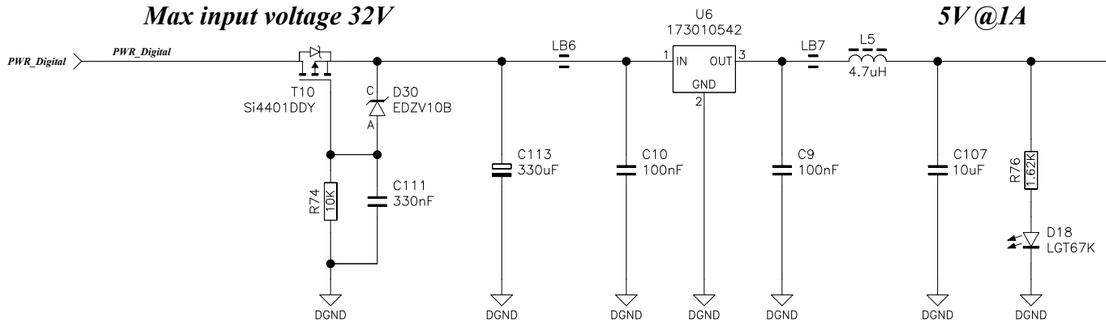
Max voltage 6V5

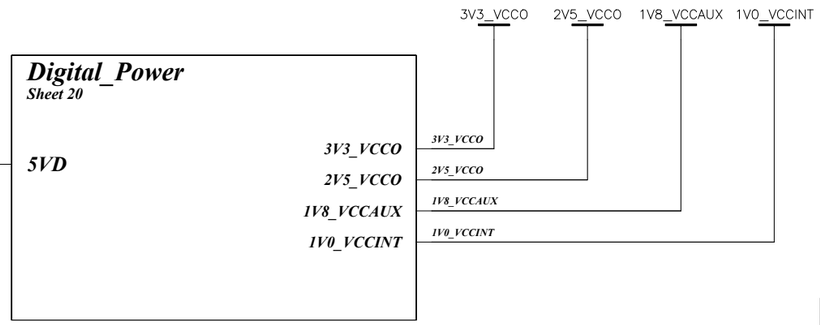




Max input voltage 32V

5V @1A





rev.	by	notes

100MHz in the loop

Project : ***ET Pathfinder demonstrator***

Sheetname : ***Power***

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Size ***420 x 297mm*** ***A3***

Sheet ***18 of 20***

Date ***2021-08-23***

Analog Domain

Vin 6V5

PWR_Vanalog_Prot → LB11 → L6 4.7uH → PWR_Vanalog_Fil

C109 10uF, C29 100nF, C108 10uF — AGND

D14 MSE1PB

U15 TPS7A47

C27 100nF, C147 1uF — AGND

C25 100nF, C171 22uF, C172 22uF — AGND

R78 1.62K

D25 LGT67K

5V_PLL → TP8 True, TP9 True

D13 MSE1PB

U14 TPS7A47

C26 100nF, C148 1uF — AGND

C28 100nF, C173 22uF, C174 22uF — AGND

R55 750

D26 LGT67K

3V3_PLL → TP6 True, TP7 True

D15 MSE1PB

U16 TPS7A47

C30 100nF, C149 1uF — AGND

C31 100nF, C175 22uF, C176 22uF — AGND

R54 750

D27 LGT67K

3V3_RESAMPLERS → TP10 True, TP11 True

rev.	by	notes

100MHz in the loop

Project	: ET Pathfinder demonstrator
Sheetname	: Power_Analog

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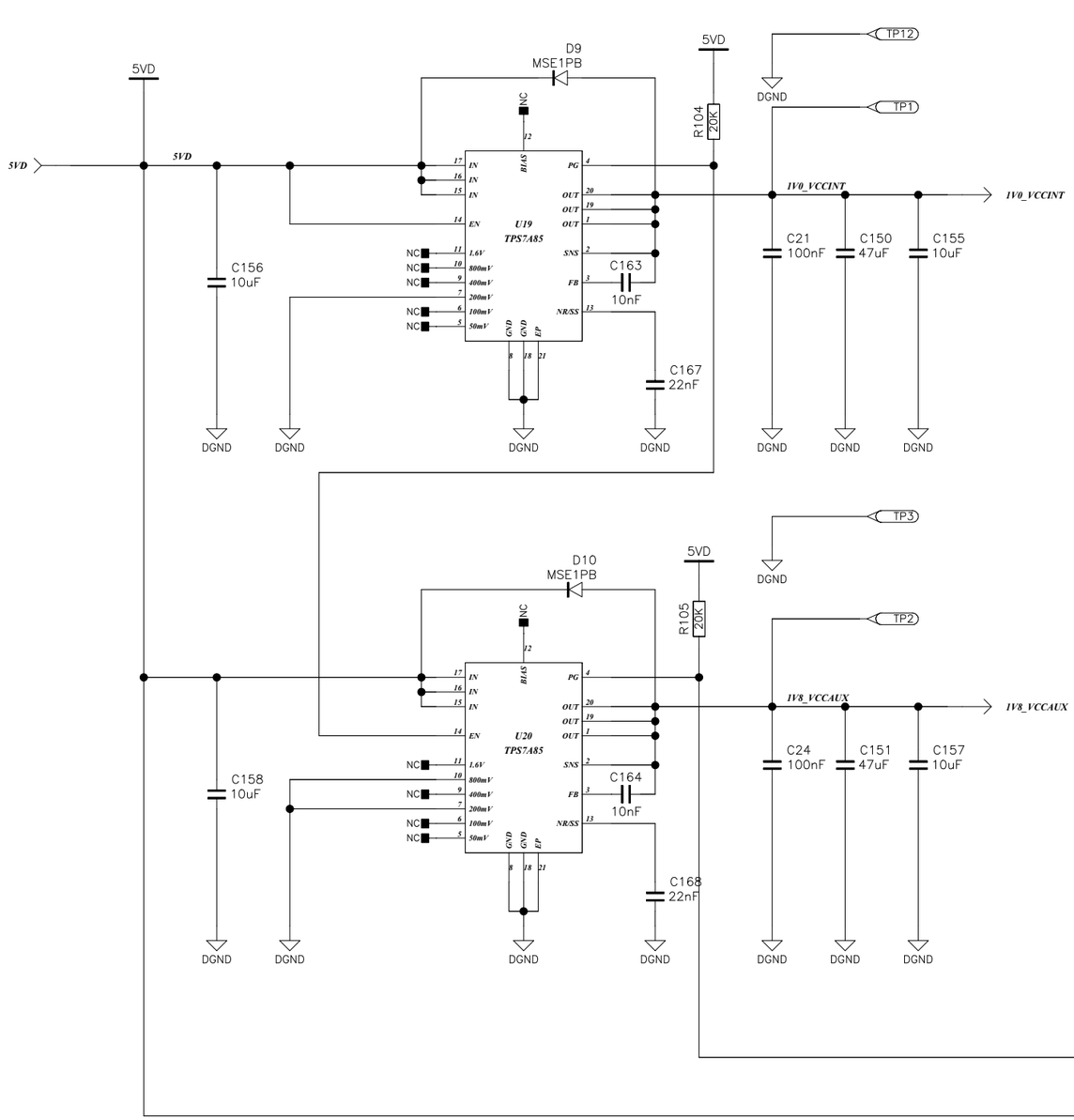
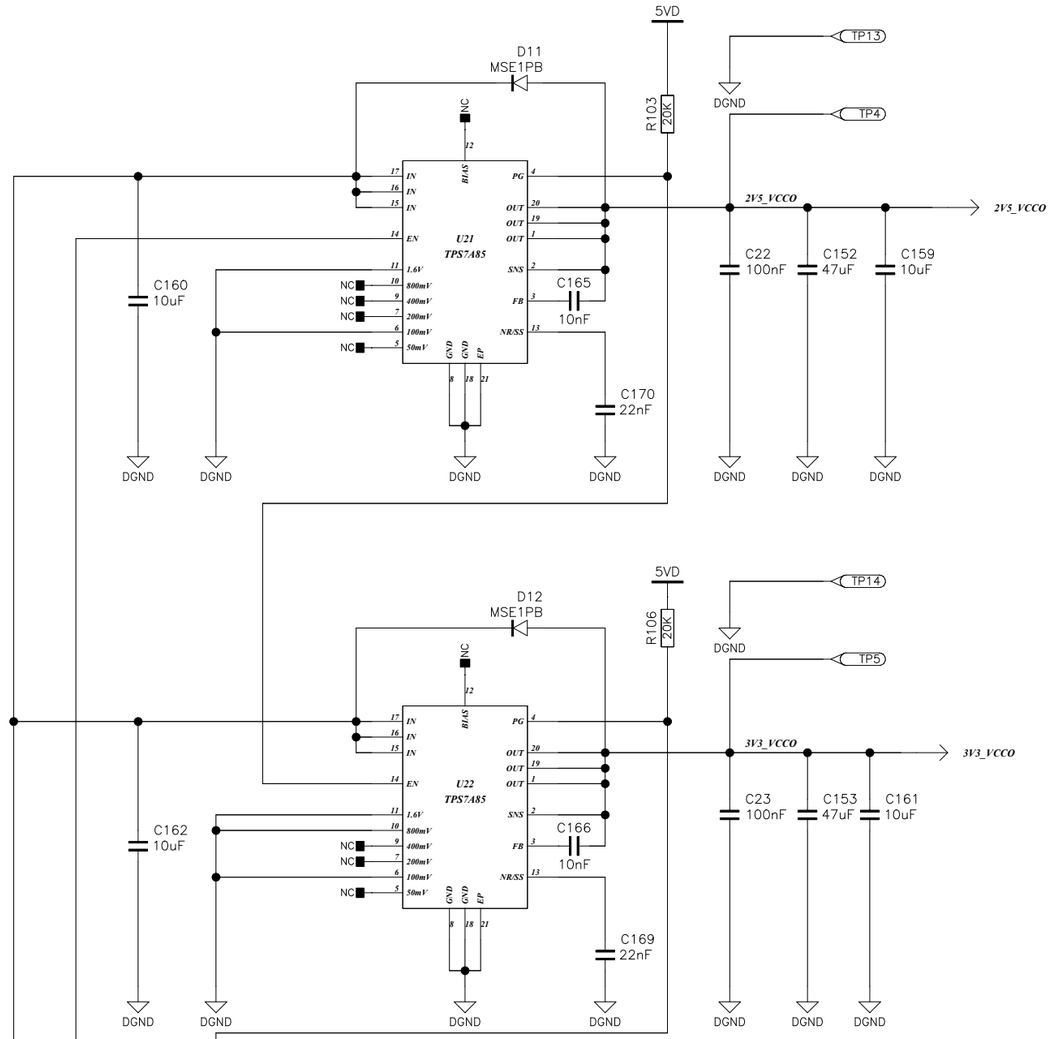
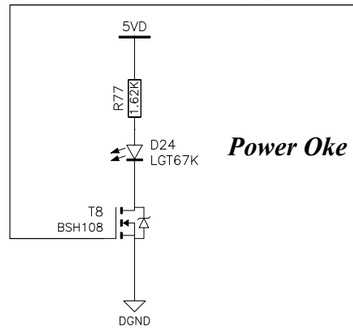
Size	420 x 297mm
Sheet	19 of 20 — A3
Date	2021-08-23







Power Oke

Powersupply for the FPGA.
The generated rail voltages are sequenced.
Sequence: 1V0 > 1V8_AUX > 2V5_VCCO > 3V3_VCCO

rev.	by	notes

100MHz in the loop

Project : ***ET Pathfinder demonstrator***

Sheetname : ***Digital_Power***

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Drawn by ***Guido Visser, Peter Jansweijer***

Size *420 x 297mm* ***A3***

Sheet *20 of 20*

Date ***2021-08-23***