ISOTDAQ Lab 14

System on Chip (SoC) FPGA

Proposal by

- Manoel Barros Marin (CERN)
- Elena Sorina Lupu (EPFL)

Manpower and tasks

- Manoel Barros Marin (CERN):
  – general lab layout, hardware integration and FPGA firmware
- Elena Sorina Lupu (EPFL):
  – uC firmware and embedded Linux, (interested in) hardware and FPGA firmware
- Andrea Borga:
  – general lab layout, documentation and exercise guidelines
- Peter Jansweijer:
  – general lab layout, moral support to Andrea (and back-up)
- Ton Damen:
  – mirroring of the system for integration at Nikhef (TBD time and effort until Dec)
  – can help is the linux part of the lab
  – can expand the lab after ISOTDAQ for the purpose

Hardware platform – done

Platform selection: Xilinx Zynq board, to be proposed by Sorina, and confirmed by all.

Reason behind Xilinx: we all love Xilinx... 8.)
Nikhef has a particular interest in the Zynq architecture for future reuse and exploration.
Andrea and Peter better prepared (or less ignorant) and used to the vivado and EDK stuff.

According to Sorina:

- Xilinx better documentation for Real Time application
- Altera better Linux documentation

Idea of the lab rev 0.1

1. use the embedded micro controller to make an LED (RGB) blink
2. use the full Linux stack to make an LED (RGB) blink
3. choose which logic peripherals should connect to the uC:
   - counter in logic up/down in multiple steps?
   - Something that suggests “co-processing”?

Future thoughts:

1. Is the use of a display easier or more effective than the LED? (print temperature for example)
2. readout a temperature sensor (ADC) and drive RGB LED with consistent temperature/colour (or brightness)
3. make a producer/consumer (client/server) on each board and make the communicate with each other
4. when is a real time OS needed and when not? Make students understand the difference between “real time” and not
5. implement a simple web server

Roadmap

- All: agree on the HW functionality first and write general specs (see idea of the lab above)
- Sorina:

        - ~~propose HW platform~~
        - choose uC example programs (reuse as much as possible)
        - choose a Linux example design suitable for the job
- Manoel, with input from Sorina:
    - setting up SoC (template, GUI clicking process)
    - pick user logic modules
    - What to do with the modules? (LEDs, ADCs, GPIO, pushbuttons)
    - How to communicate? (AXI bus?)
- Andrea/Peter:
    - ~~talk to Markus and purchase the equipment~~
    - keep an eye on the points above
    - ~~check possibility to get the HvA student~~
    - ~~put him on track to mirror what Manoel and Sorina are doing~~
    - ~~“use” him to kick-start documentation~~
    - see if Ton can help here on the Linux side

Timetable

We go backwards:

- 31/01/2017: lab must be ready and documented for students
- 15/01/2017: lab must be ready, documentation for tutors complete, documentation for students outlined
- Christmas: drink loads of wine to recover from the strain and stress
- 23/12/2016: lab “should do something”, documentation for tutors outlined
- 15/12/2016: check where we stand
- 01/12/2016: setup the Linux part of the lab
- 15/11/2016: check where we stand and start (or continue) setup of the uC part of the lab
- 08/11/2016: complete tool-flow setup the environment with all the clinking stuff
- 01/11/2016: we should have the boards at Nikhef, CERN, EPFL
- 19/10/2016: make hardware selection and start purchasing process
- 12/10/2016: start of the crazy suicide preparation plan

Fall back in case of total failure: make a sort of guided tour with slides and a demo driven by the tutor.
[I don't want to consider this for now...:)]

Or just say that we did our best and we keep the lab for 2018.
[this is something that I want to consider even less for now...:)]